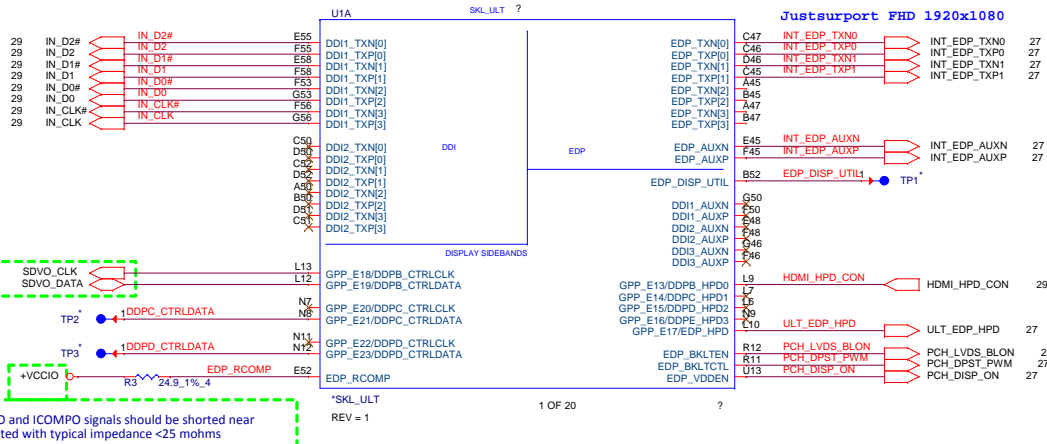


LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : IN3(High)  
LAYER 7 : SGND1  
LAYER 8 : BOT

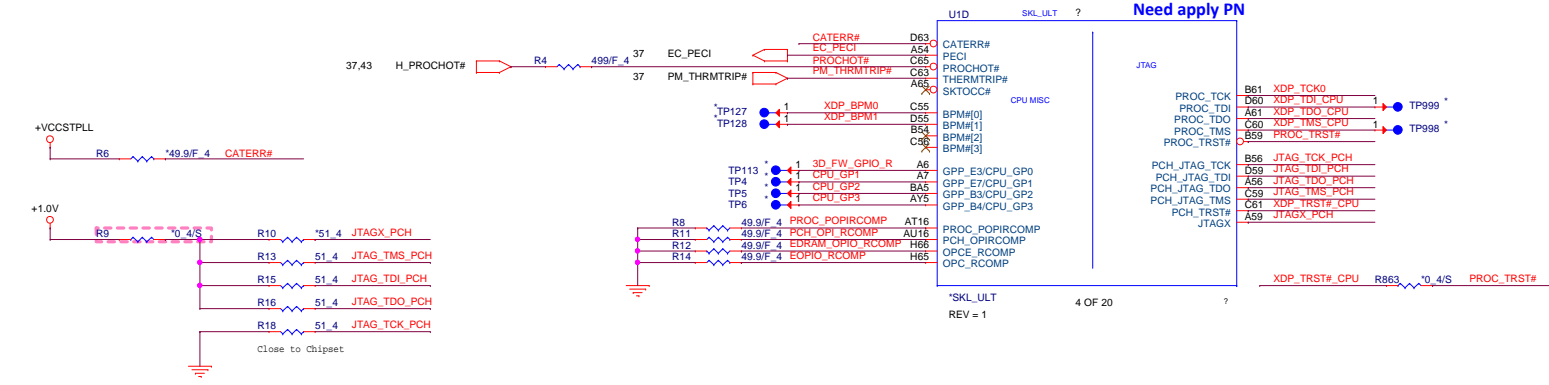
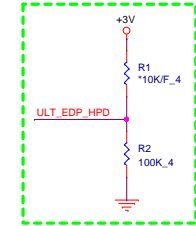


+3V 4,10,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,35,36,37,43,46,51  
+1.0V 4,6,37,42  
+VCCSTPLL 4,5,6,9,42,43

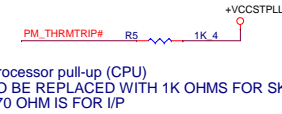
## HDMI



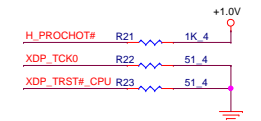
Reserve EDP\_HPD opposites circuit!



Close to EC



PLACE NEAR CPU



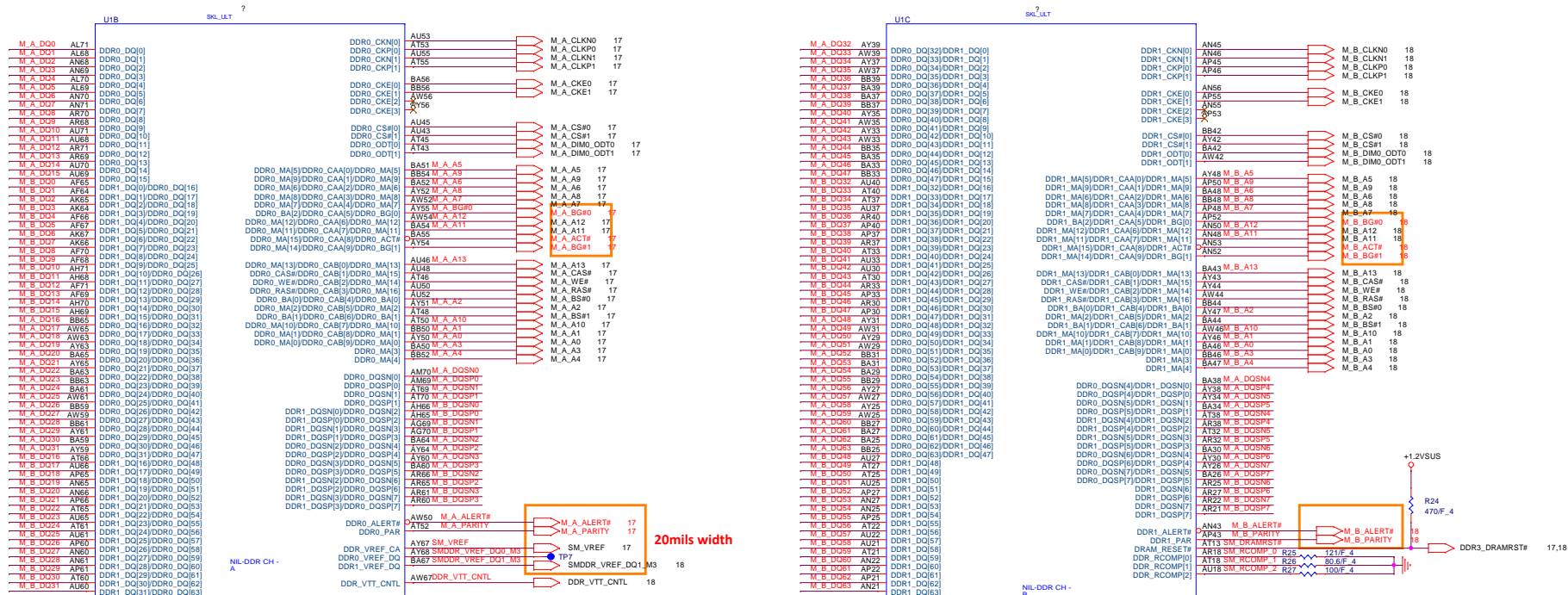
**PROJECT : G74A**  
**Quanta Computer Inc.**

Size Custom Document Number 02 -- SKYPAKE 1/15 (eDP/DDI) Rev 1A  
Date: Wednesday, January 11, 2017 Sheet 2 of 51

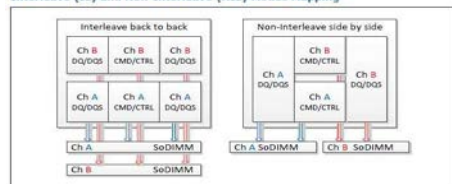
## SkyLake ULT Processor (DDR4)

17 M\_A\_DQSN[7:0]  
17 M\_A\_DQSP[7:0]  
18 M\_B\_DQSN[7:0]  
18 M\_B\_DQSP[7:0]  
17 M\_A\_DQ[63:0]  
18 M\_B\_DQ[63:0]

+1.2V<sub>SUS</sub> 6,17,18,40,42,48

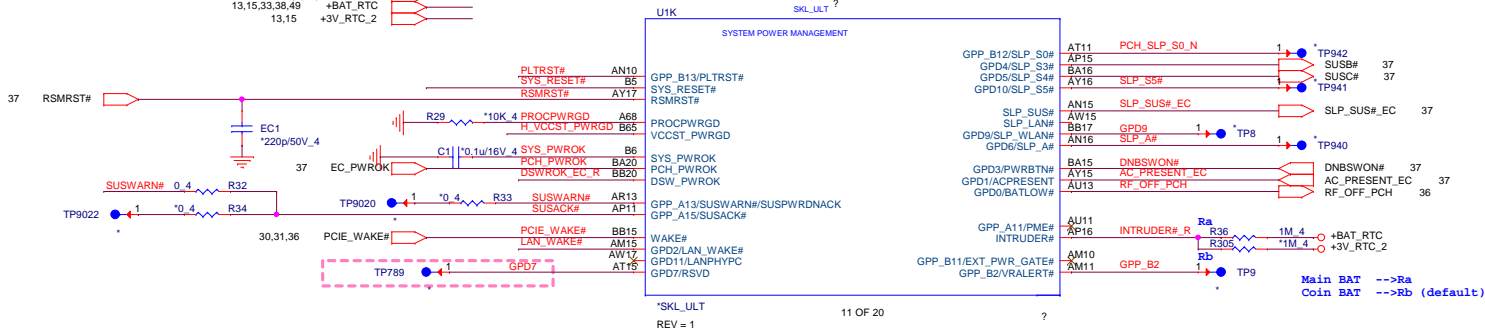
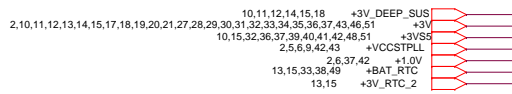


Interleave (IL) and Non-Interleave (NIL) Modes Mapping

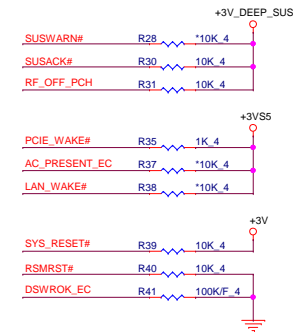


PROJECT : G74A  
Quanta Computer Inc.

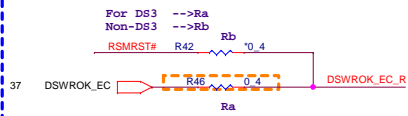
Size Custom Document Number 03 - SKYLAKE 2/15(DDR4 I/F) Rev 1A  
Date: Wednesday, January 11, 2017 Sheet 3 of 51



## PCH Pull-high/low(CLG)

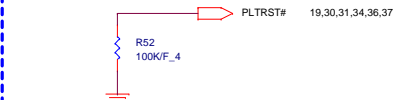


## For DS3 Sequence

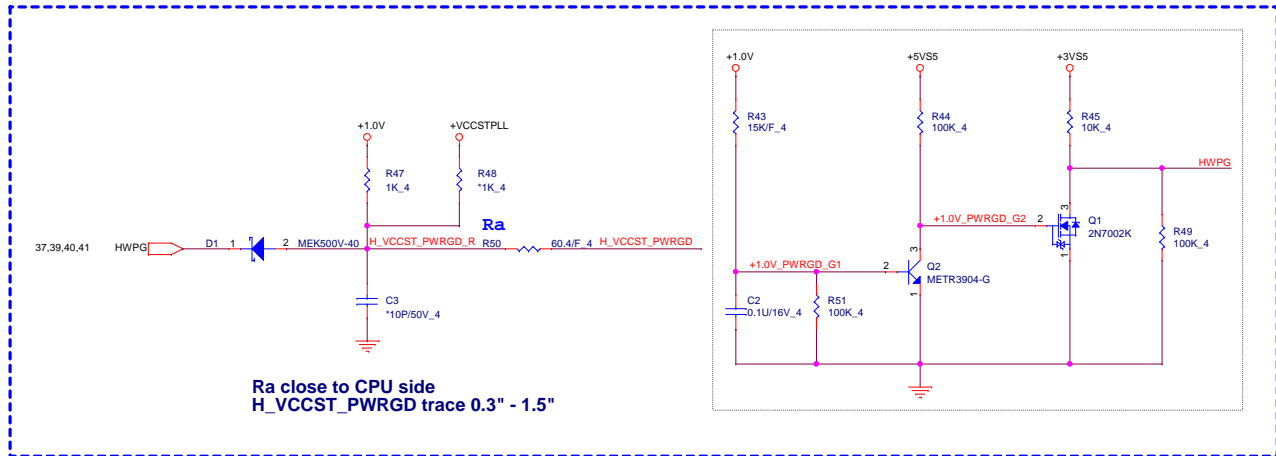
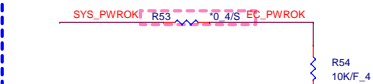


## PLTRST#(CLG)

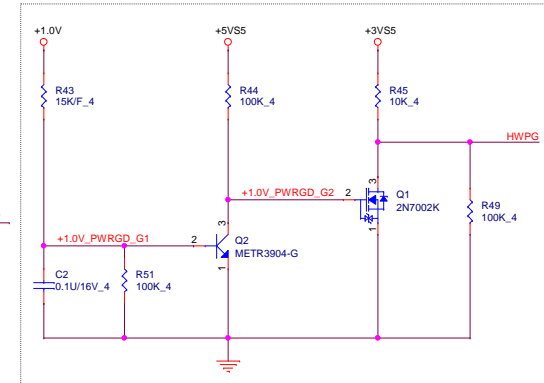
Check Rise/Fall time less than 100ns

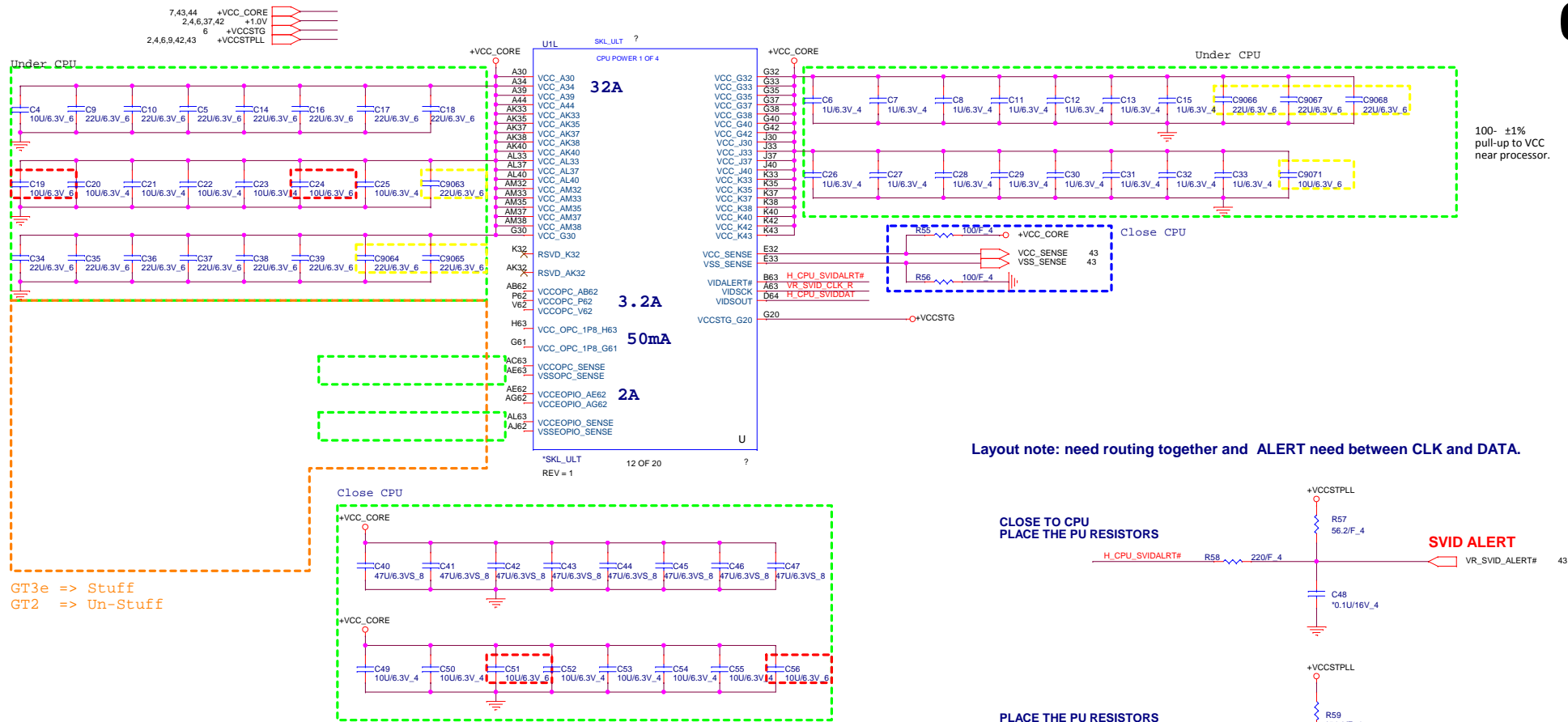


## System PWR\_OK(CLG)

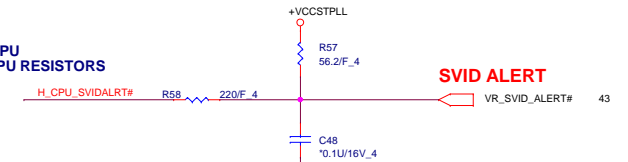


Ra close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"

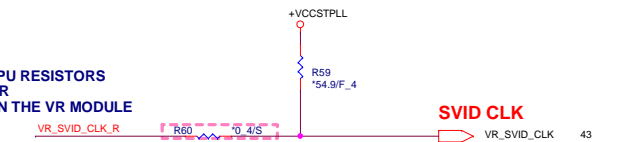




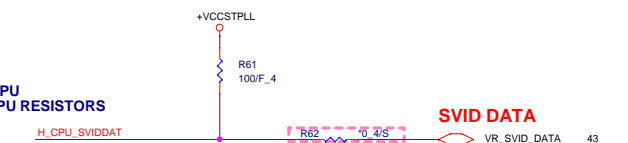
CLOSE TO CPU  
PLACE THE PU RESISTORS



PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE

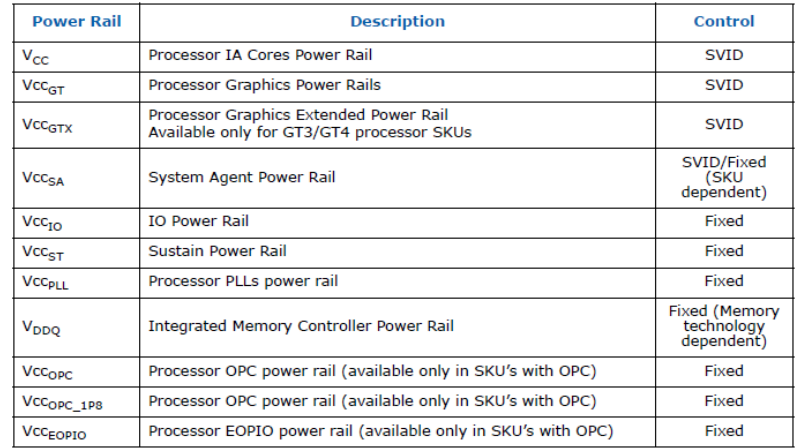


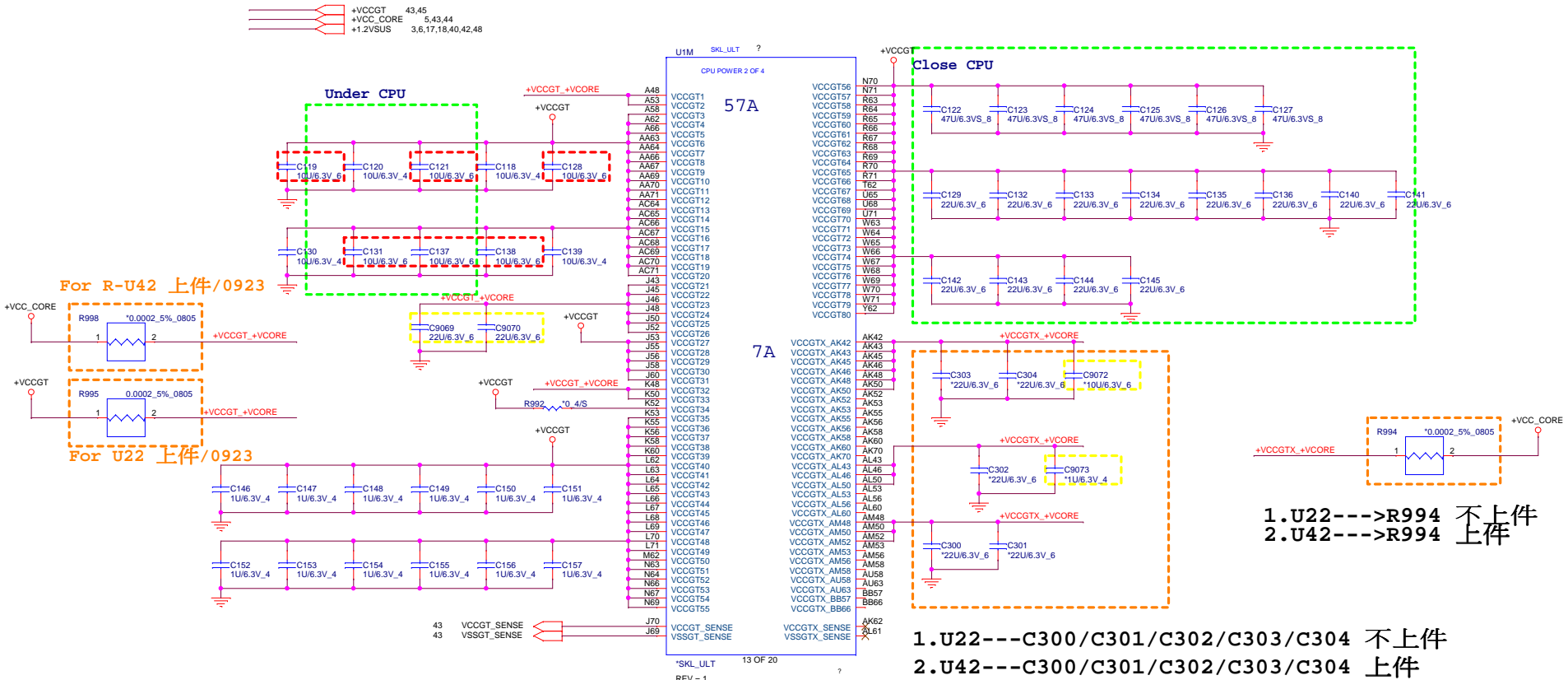
CLOSE TO CPU  
PLACE THE PU RESISTORS



**PROJECT : G74A**  
**Quanta Computer Inc.**

Size Custom Document Number 05 -- SKYLAKE 4/15 (POWER-1) Rev 1A  
Date: Wednesday, January 11, 2017 1 Sheet 5 of 51

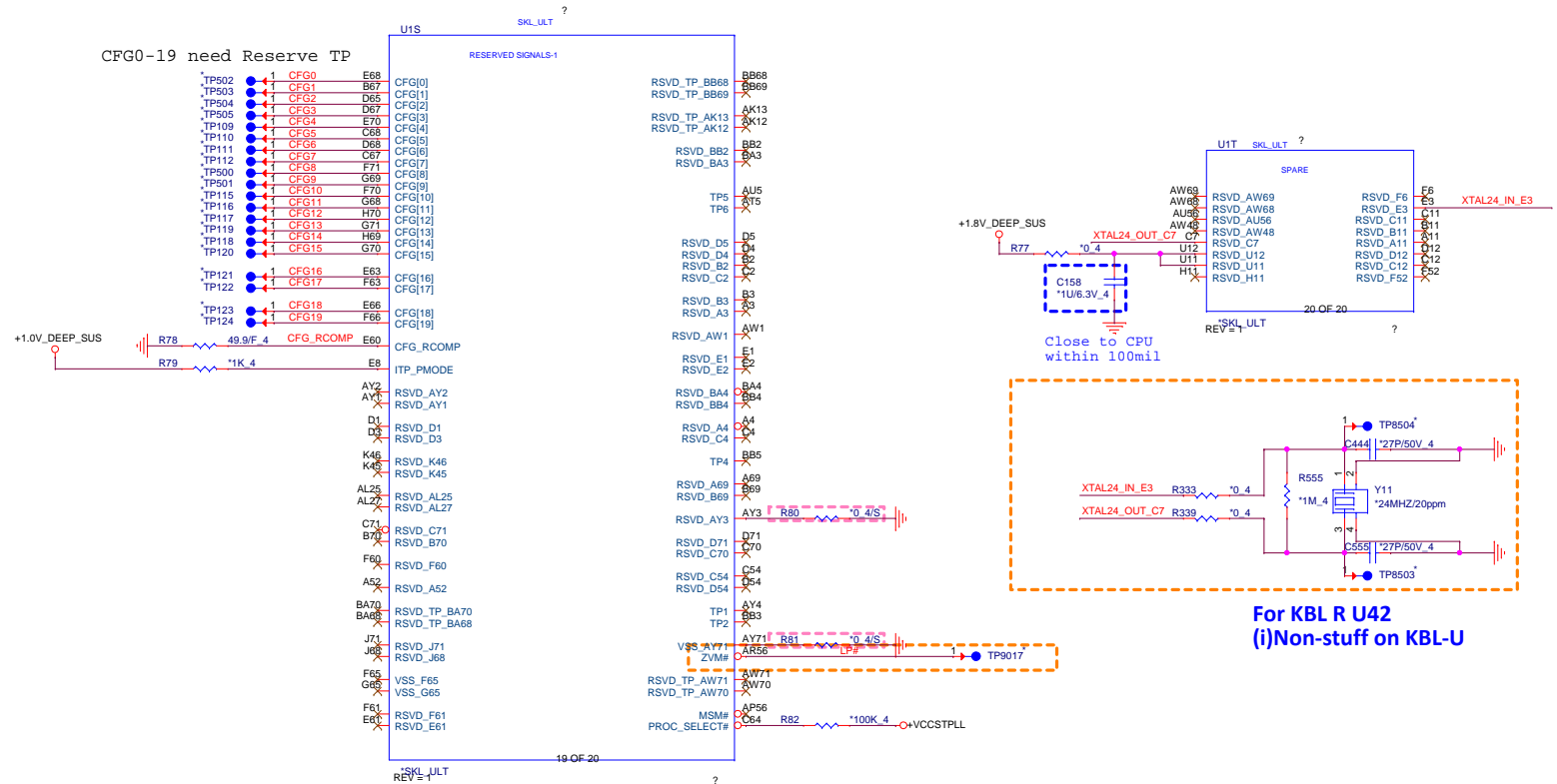




Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1PB</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



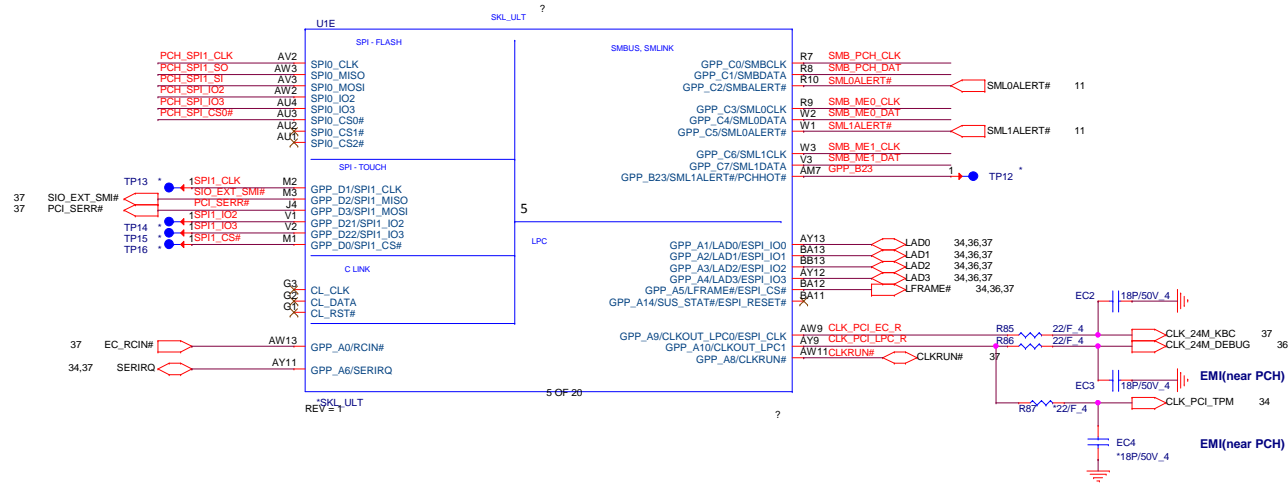




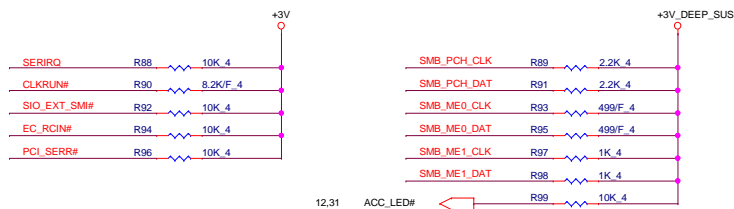
**Processor Strapping** The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable: No physical DP attached to eDP	Enable: An ext DP device is connected to eDP	

+3V_DEEP_SUS	4,11,12,14,15,18
+3V	2,4,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,35,36,37,43,46,51
+5V	27,28,29,33,35,51
+1.0V	2,4,6,37,42
+3VS5	4,15,32,36,37,39,40,41,42,48,51



## GPIO Pull UP



## PCH SPI ROM(CLG)

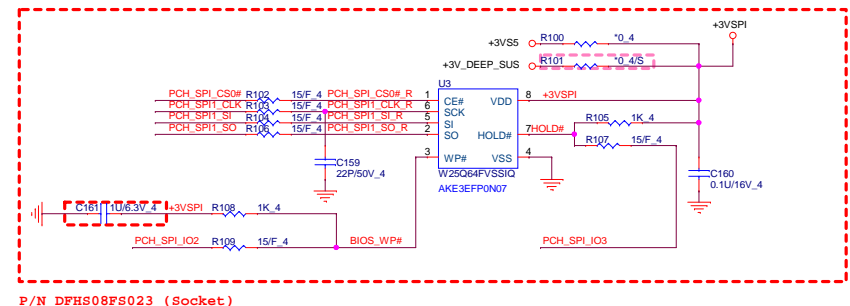
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023



need place to TOP

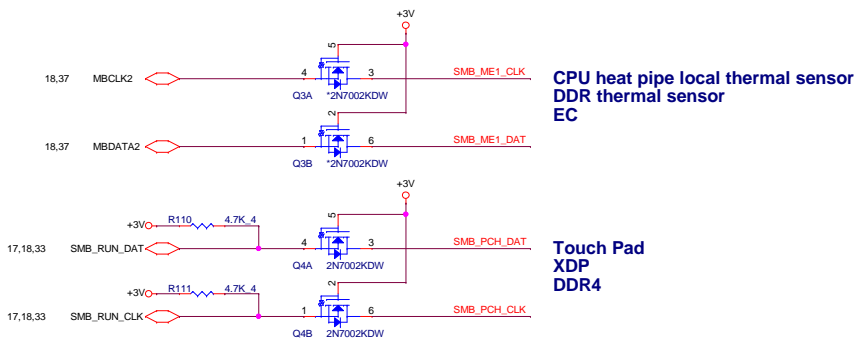
TP size TP2675

## PCH SPI ROM(CLG)



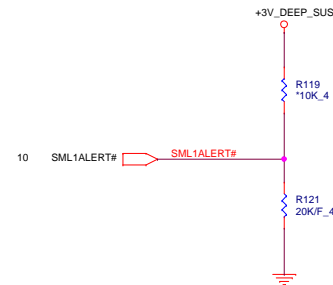
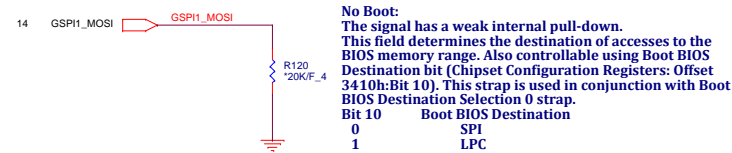
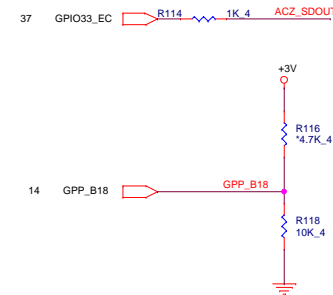
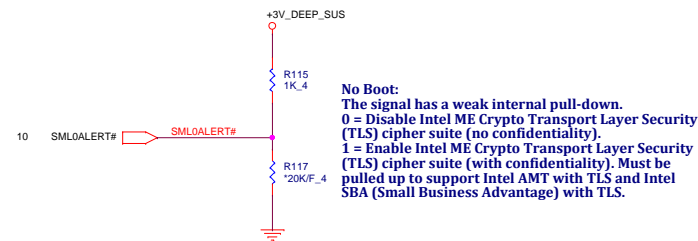
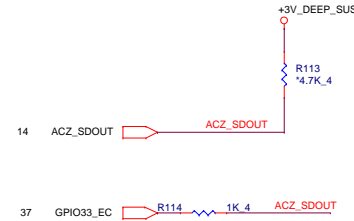
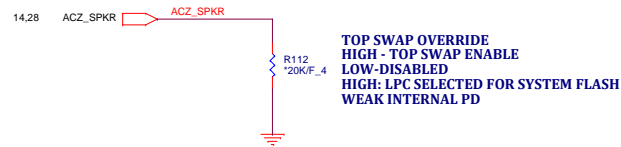
P/N DFHS08FS023 (Socket)

## SMBus/Pull-up(CLG)



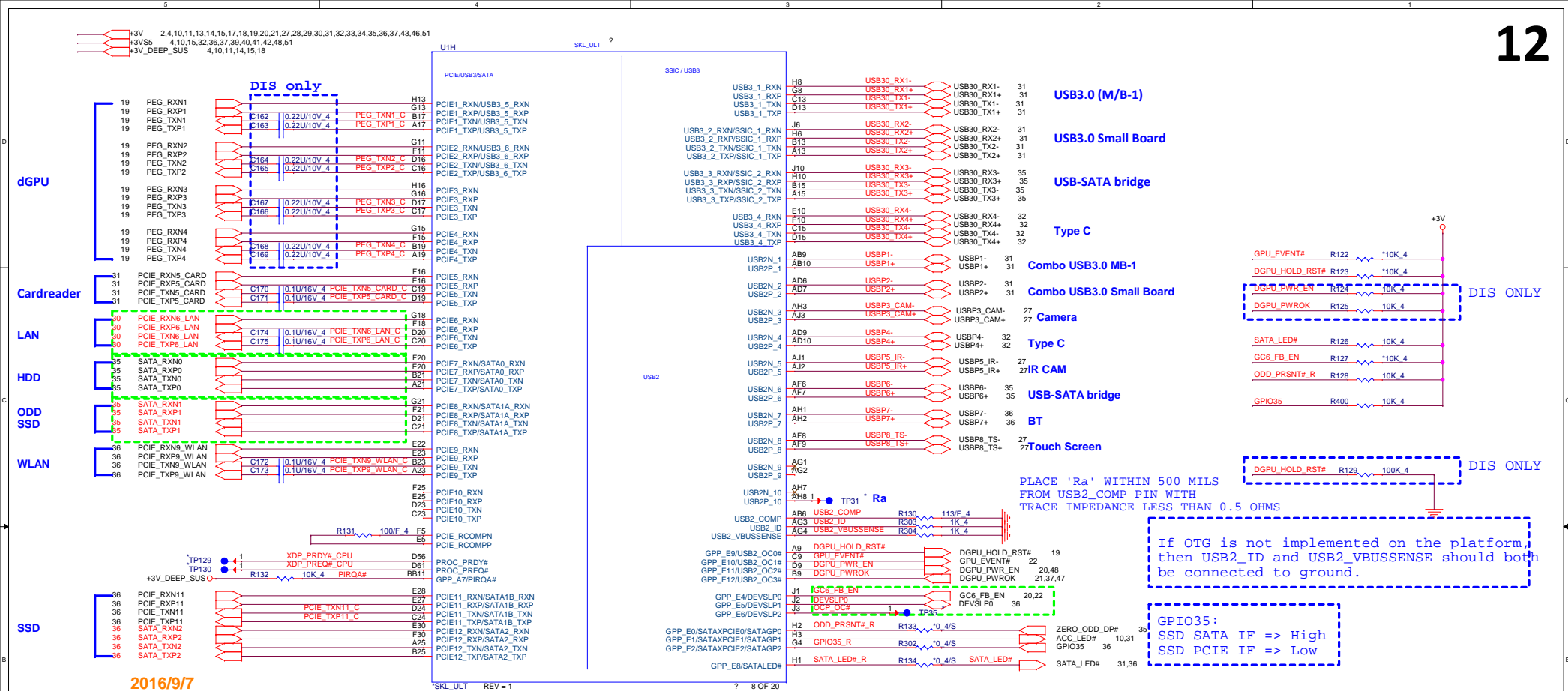
# Functional Strap Definitions

**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



**PROJECT : G74A**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>11 -- SKYLAKE 10/15(HDA)</b>	Rev 1A
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2016/9/7  
For Base-U the SATA1B/SATA2 delete

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	CR
Port3	dGPU	Port2	SSD
Port4	dGPU	Port3	WLAN
Port5	CardReader	Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8	SSD		
Port9	WLAN		
Port10	Un-used		
Port11	SSDx2		
Port12	SSDx2/ SATA2		

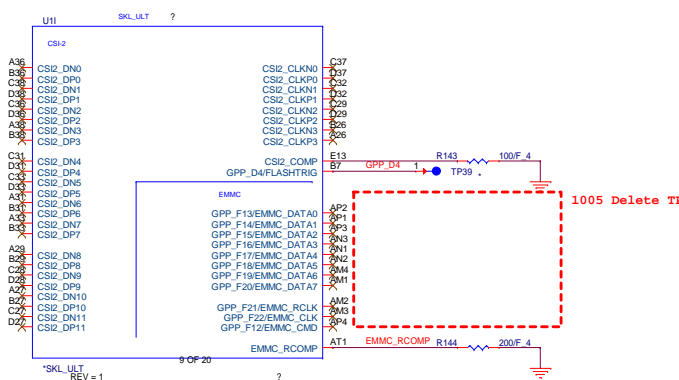
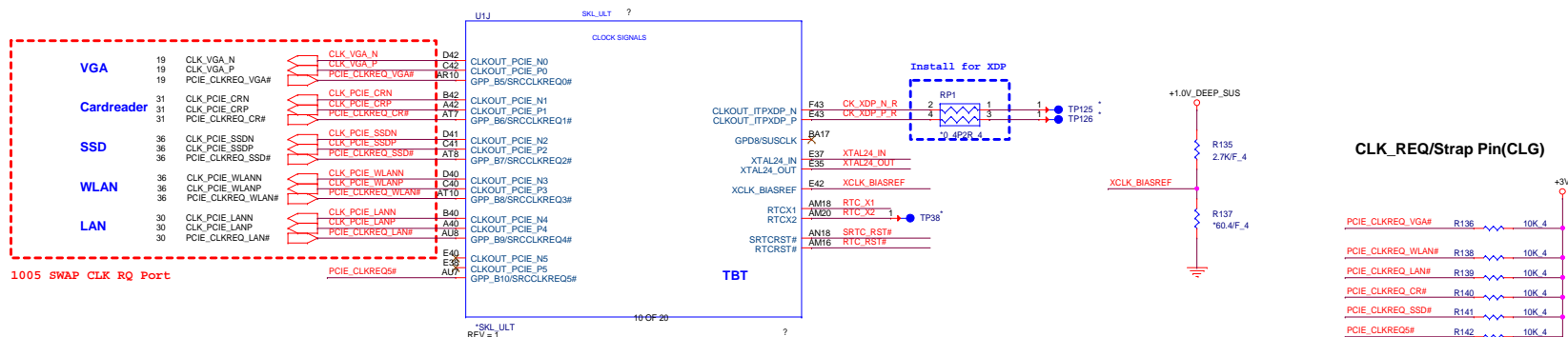
USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 Small Board
PORT-3	USB-SATA bridge
PORT-4	Type C

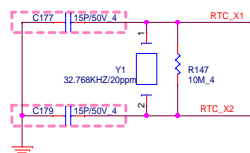
USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	Camera
PORT-4	Type C
PORT-5	IR CAM
PORT-6	USB-SATA bridge
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

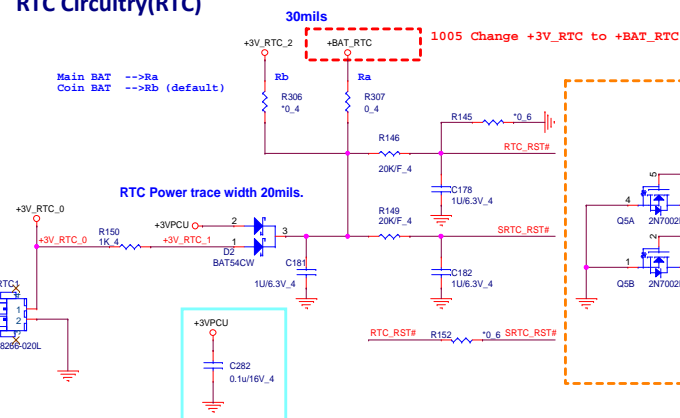
-3V\_RTC\_2 4,15  
 -BAT\_RTC 4,15,33,38,49  
 -1.6V\_DEEP\_SUS 9,15,41  
 -3V 2,4,10,11,12,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,35,36,37,43,46,51



## RTC Clock 32.768KHz

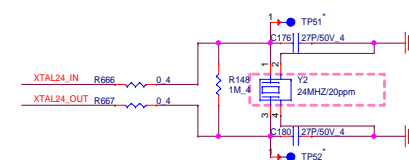


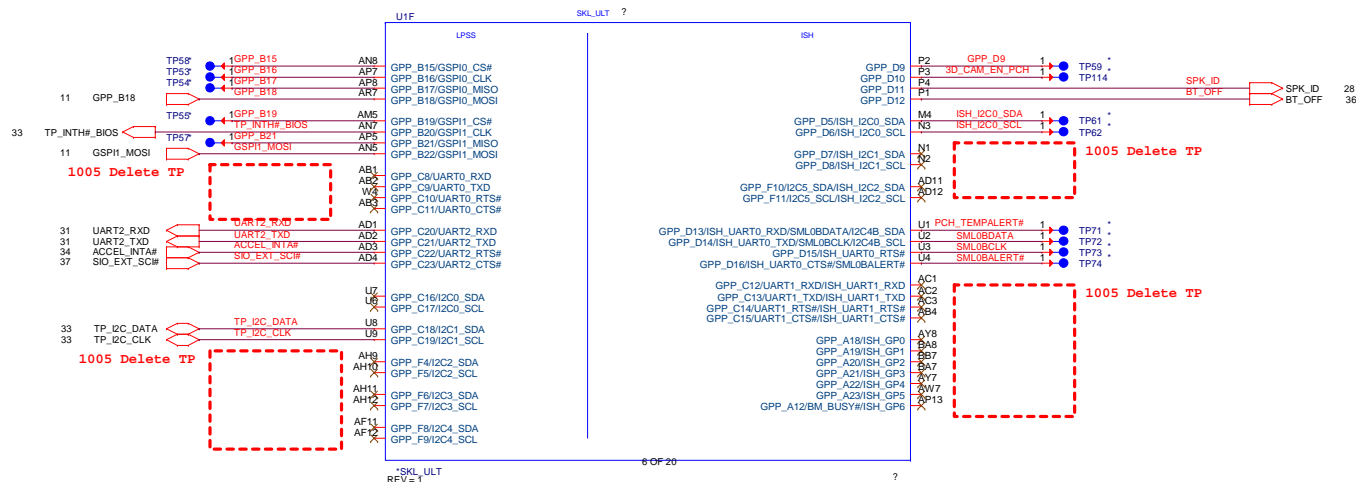
## RTC Circuitry(RTC)



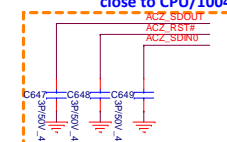
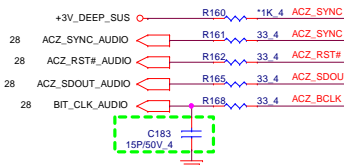
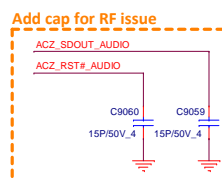
## External Crystal

The 24 Mhz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 Mhz (30 Ohm ESR) XTAL for Cannonlake-U.

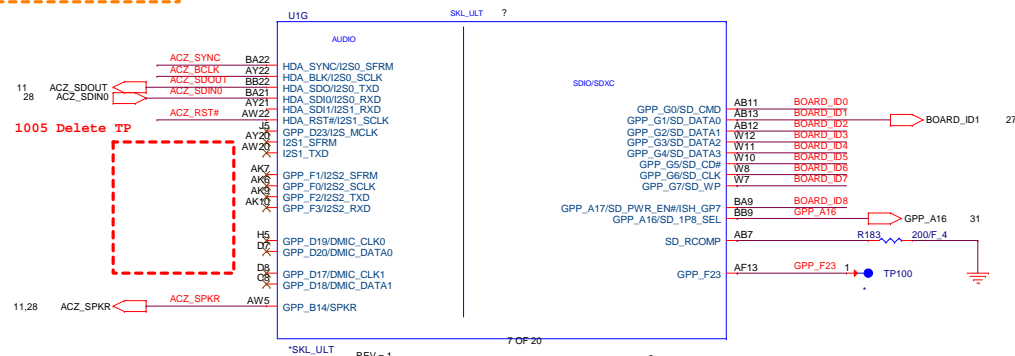




close to CPU/1004



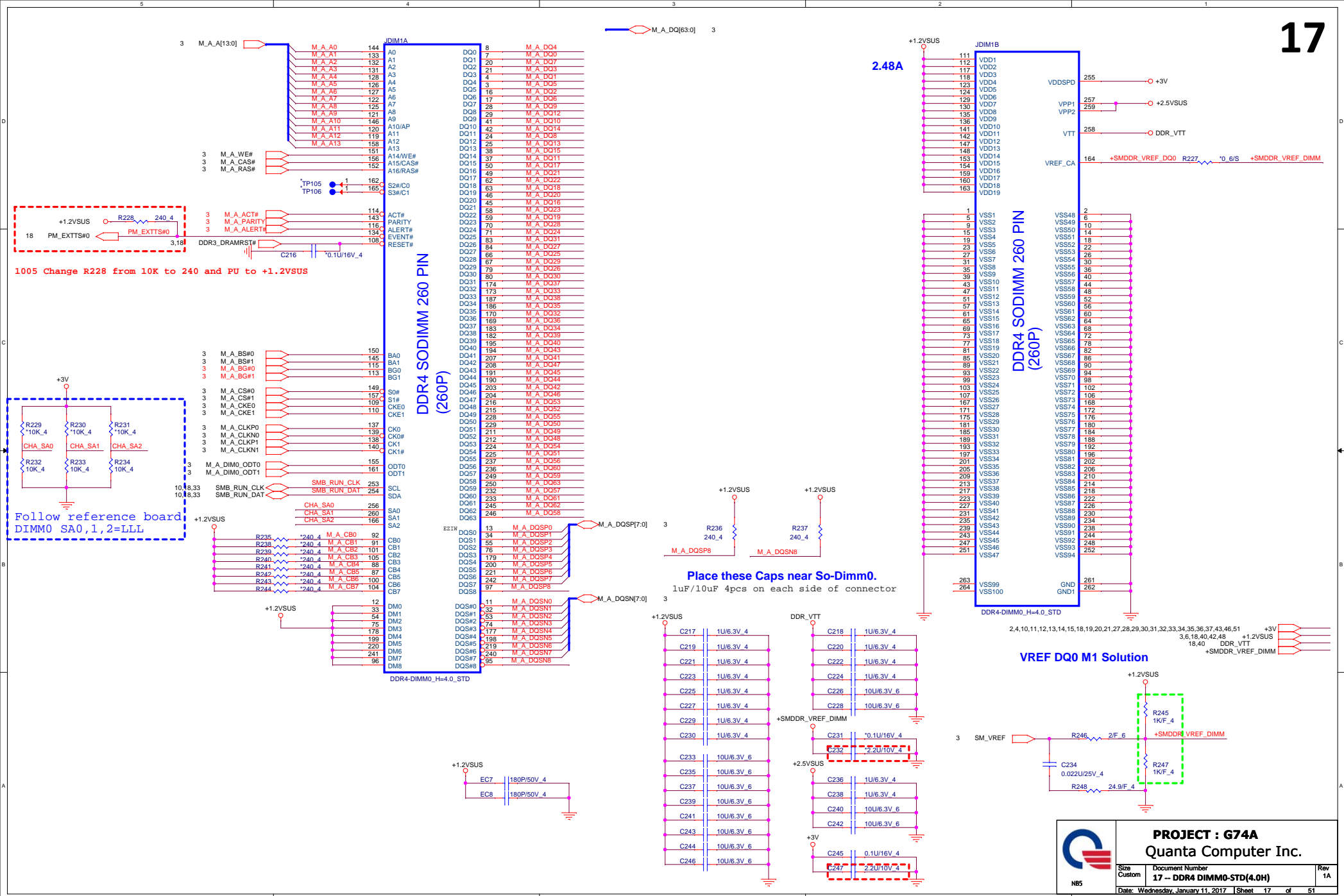
Skylake U	BOARD_ID[8:7]	Board ID 6	Board ID 5	Board ID 4	Board ID 3	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6	ID5	ID4	ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 0)	0 : AMD 1 : Nvidia GPU setting	0 : 4VRAM 1 : 8VRAM	0 : VGA CAM 1 : IR CAM	00 : 14" 01 : 15 1SPD 10 : 17" 11 : 2SPD	0 : UMA 1 : DIS

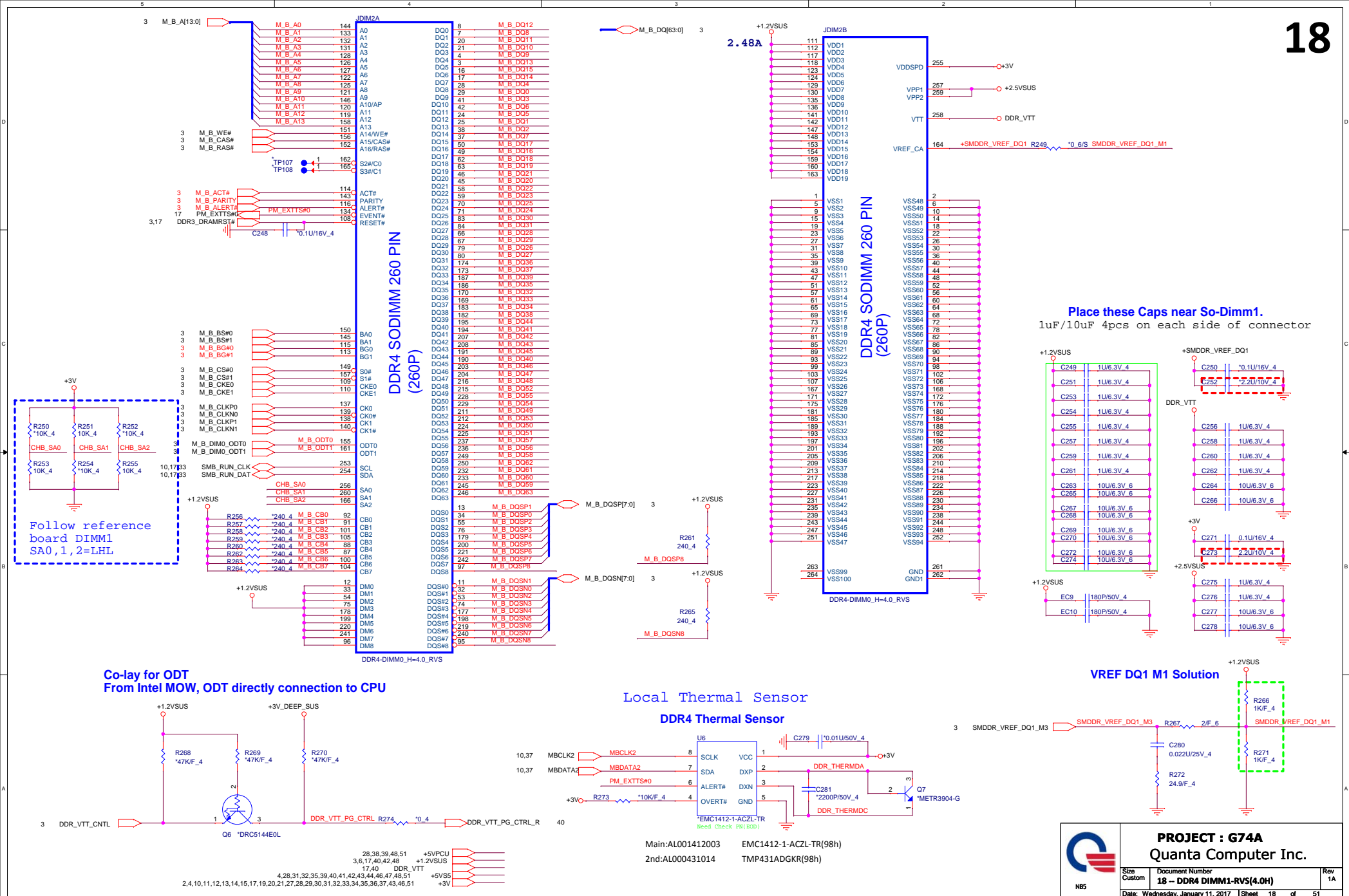








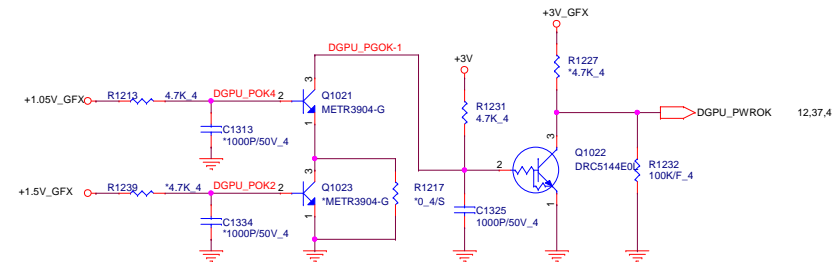
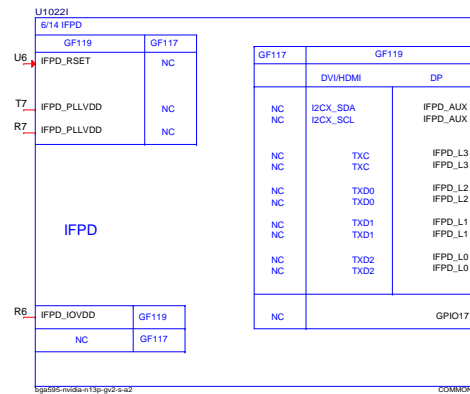
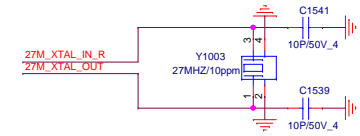
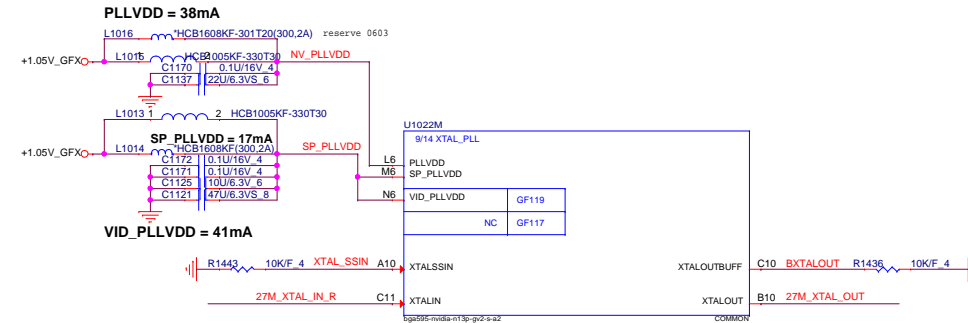
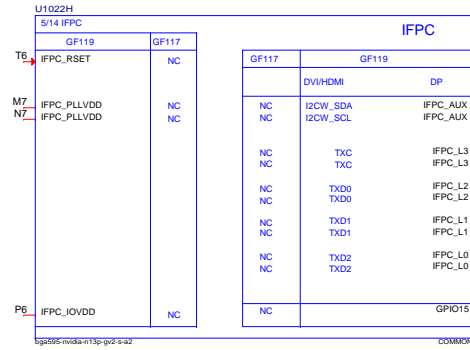
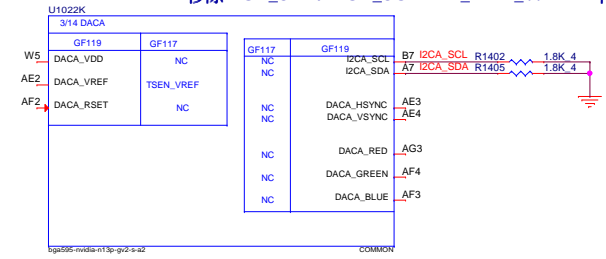
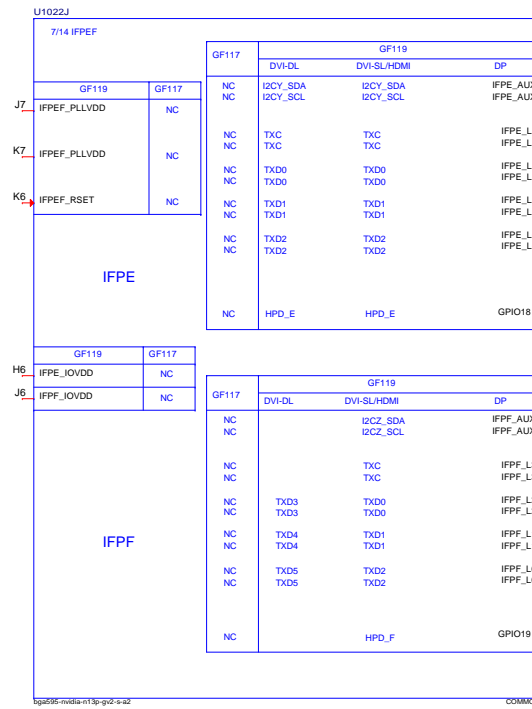
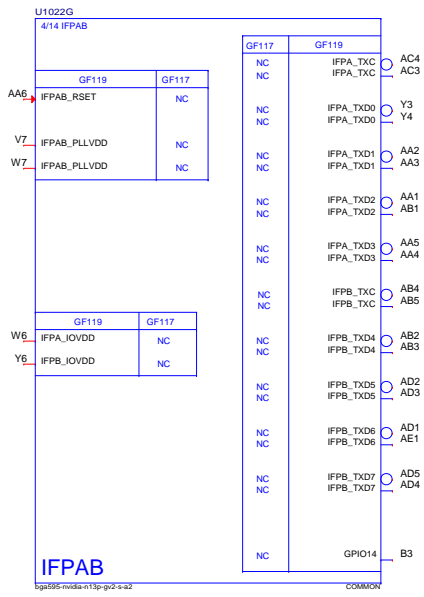


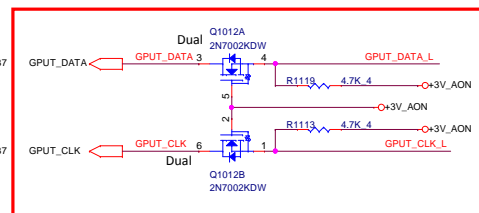
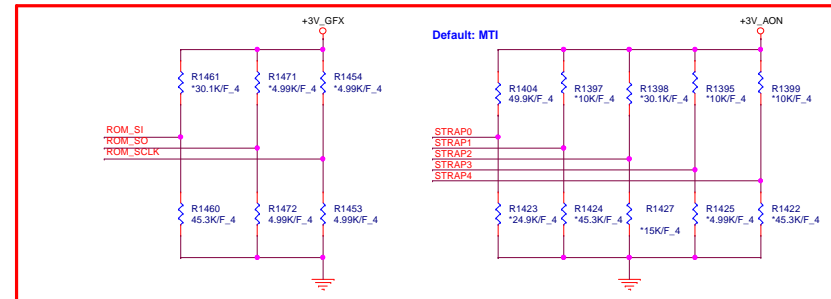






移除I2CA\_SDA/ I2CA\_SCL MIN\_LINE\_WIDTH 內的數值。





Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

RAMCFG [3..0]	DESCRIPTION	Vendor	Vendor P/N	256Mx16 Strap	128Mx16 Strap	QBC	TOP B/S
1100	DDR3 256Mx16, 64bit, 4Gb, 1GMHz	HYNIX	H5TC4G63CFR-N0C	0XC	0x9	AKD5PZDTW02	AKD5PZDTW01
1101	DDR3 256Mx16, 64bit, 4Gb, 1GMHz	HYNIX	MT41J256GLD-091G:N	0x3	0x3	AKD5PZDTW02	AKD5PZDTW01
1111	DDR3 256Mx16, 64bit, 4Gb, 1GMHz	SAMSUNG	K4W4G1646E-BC1A	0XD	0x4	AKD5PZDTW01	AKD5PZDTW00

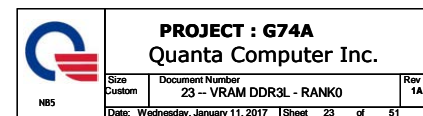
GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY_VREF CONTROL
11	OUT	PWR_VID	GPU_CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



**PROJECT : G74A**  
Quanta Computer Inc.

Size Custom	Document Number <b>22 - N16S-GT (GPIO/STRAPS)</b>	Re 1
Date: Wednesday, January 11, 2017	Sheet 22 of 51	

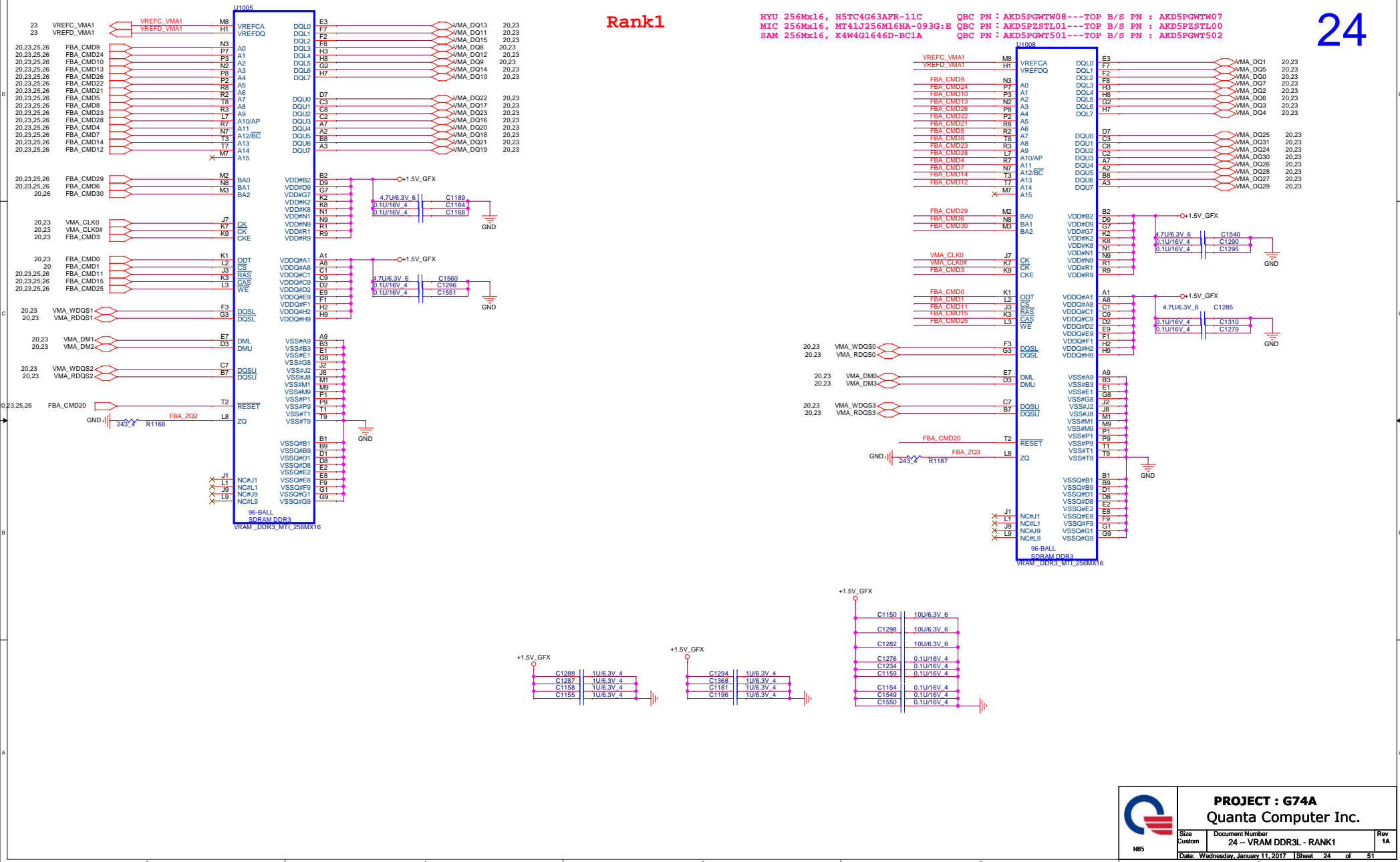




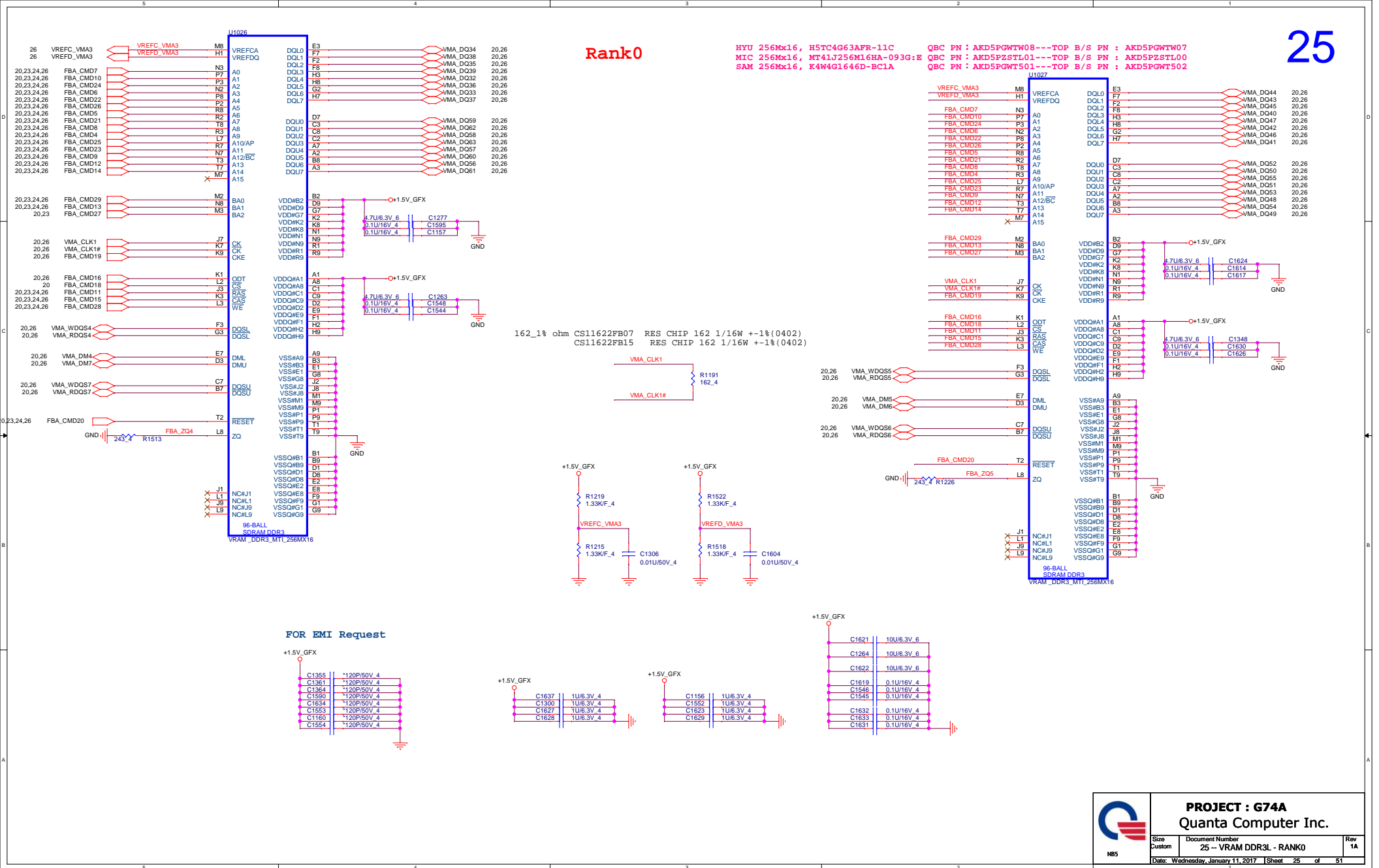
Rank1

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZ8TL01---TOP B/S PN : AKD5PZ8TL00  
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

24



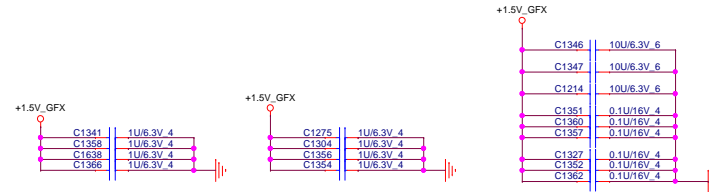
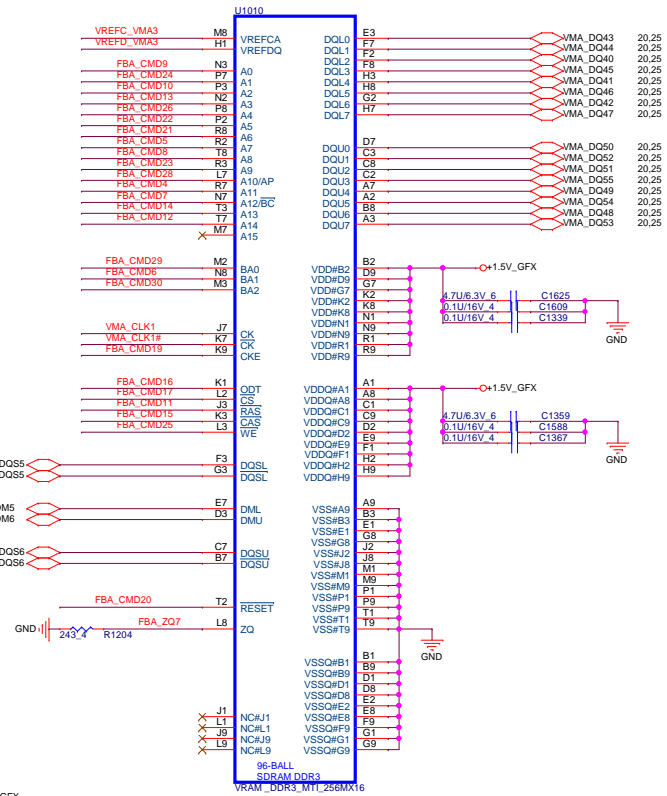
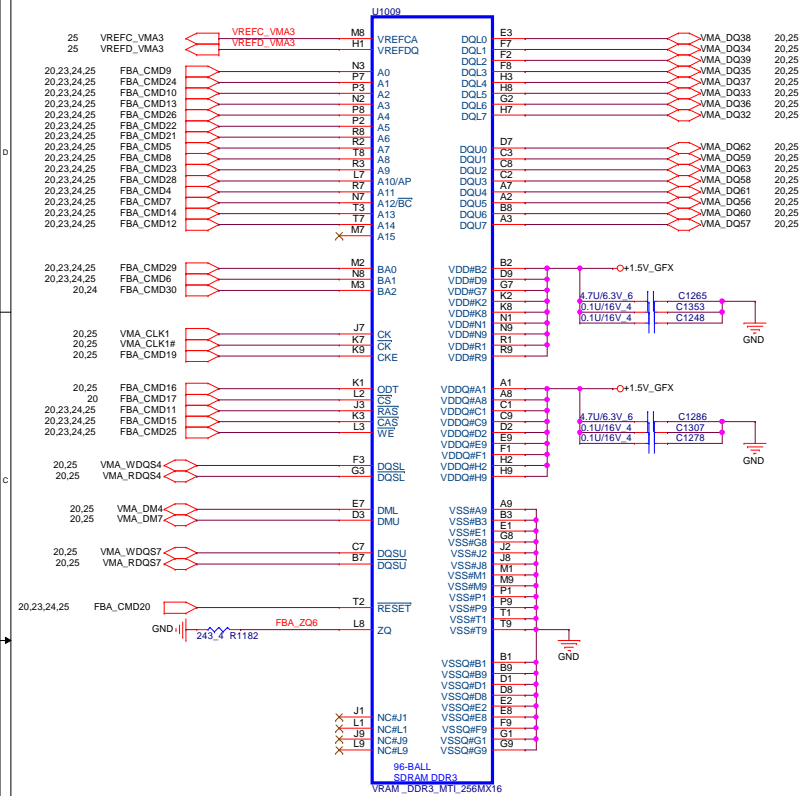




Rank1

HYU 256Mx16, H5TC4G63AFR-11C  
MIC 256Mx16, MT41J256M16HA-093G:E  
SAM 256Mx16, K4W4G1646D-BC1A

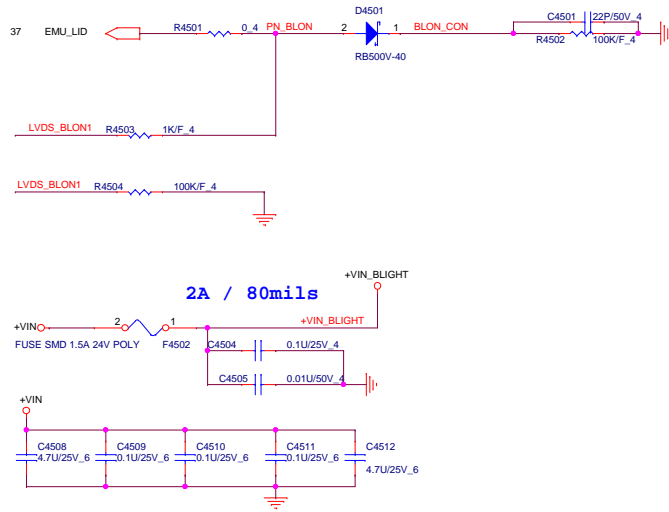
QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00  
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



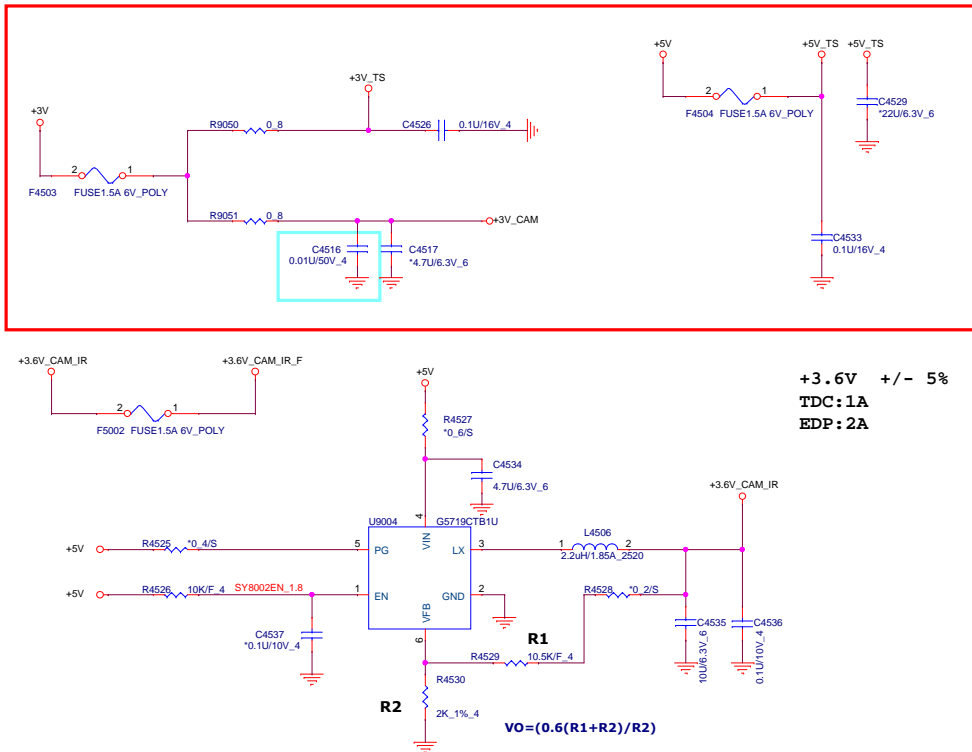
PROJECT : G74A  
Quanta Computer Inc.

Size Custom Document Number 26 - VRAM DDR3L - RANK1 Rev 1A  
Date: Wednesday, January 11, 2017 Sheet 26 of 51

## LID Switch



## Touch screen

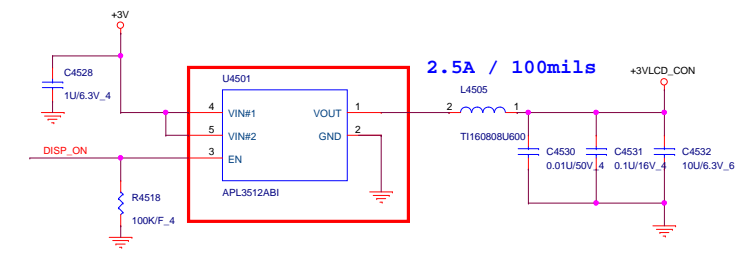
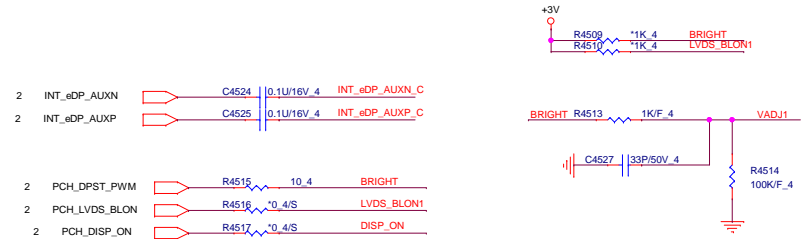
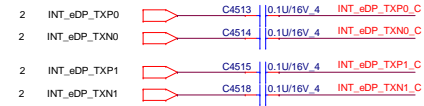
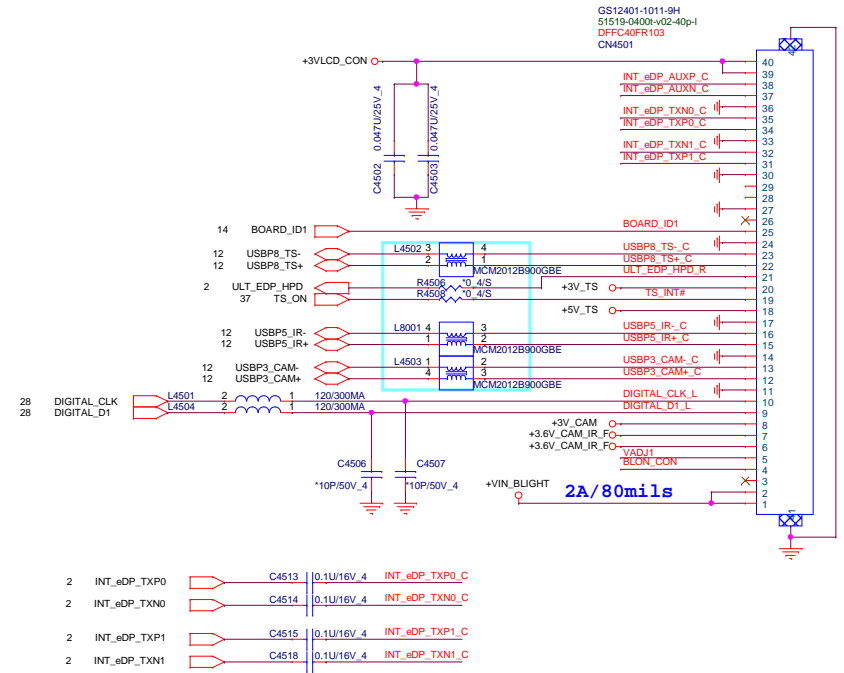


+3.6V +/- 5%  
TDC: 1A  
EDP: 2A

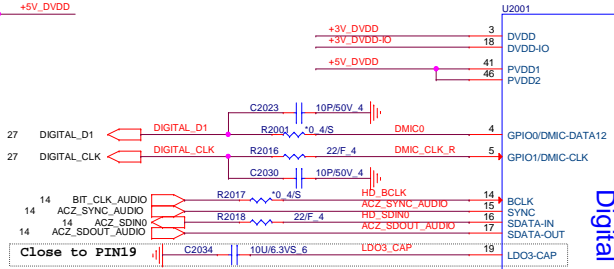
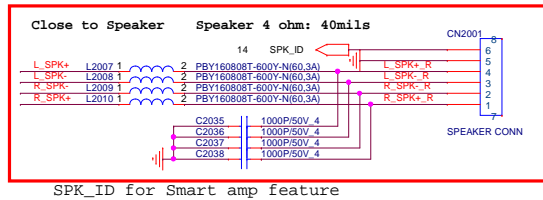
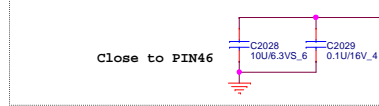
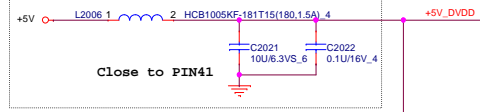
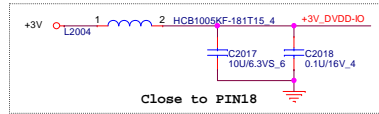
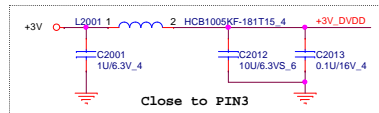
$$VO = (0.6(R1 + R2) / R2)$$

## eDP Conn.

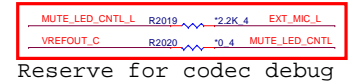
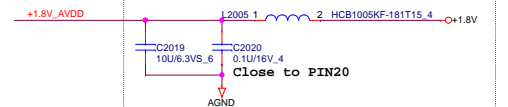
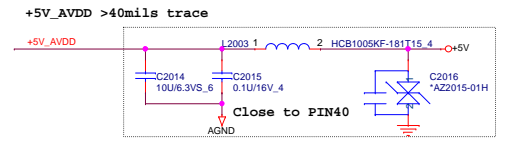
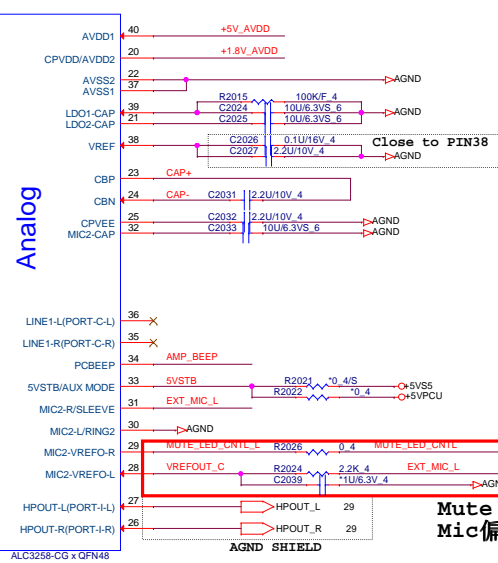
27



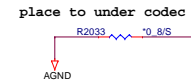
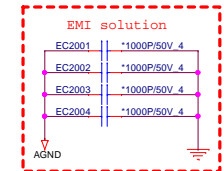
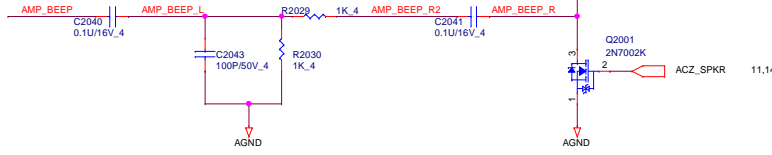
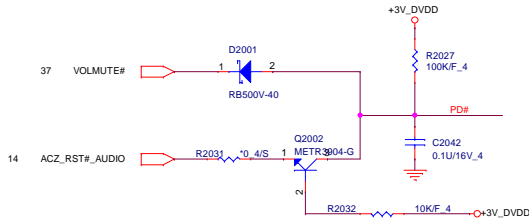
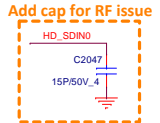
2,4,10,11,12,13,14,15,17,18,19,20,21,28,29,30,31,32,33,34,35,36,37,43,46,51  
6,13,31,32,33,36,37,38,39,49  
28,29,33,35,51  
33,35,38,39,40,41,44,45,46,47,50



Analog



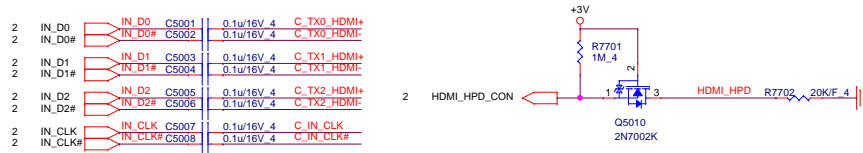
Mute LED改用Mic2-Vrefo-R  
Mic偏壓改用Mic2-Vrefo-L



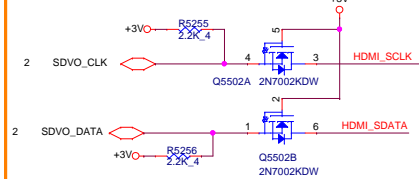
PROJECT : G74A  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	28 - Codec ALC3258-CG	1A
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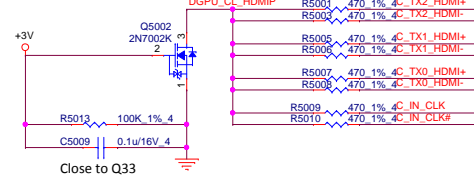
## HDMI CONN



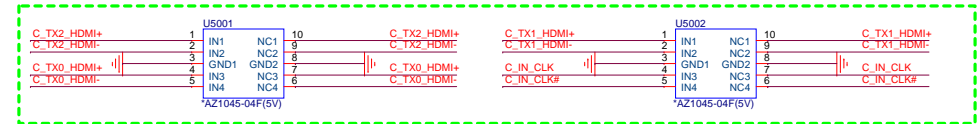
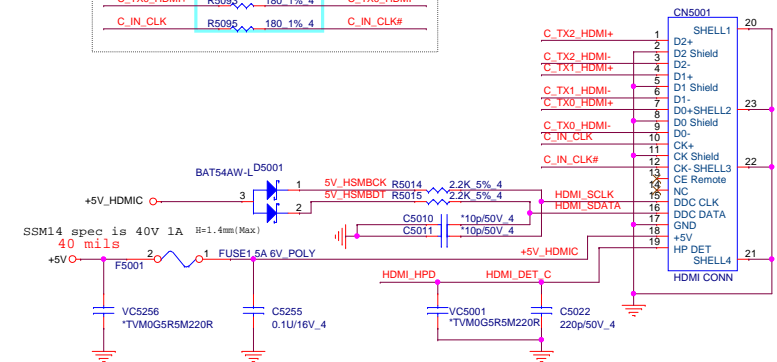
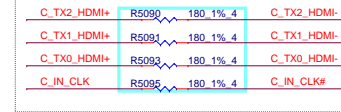
## HDMI SMBus Isolation



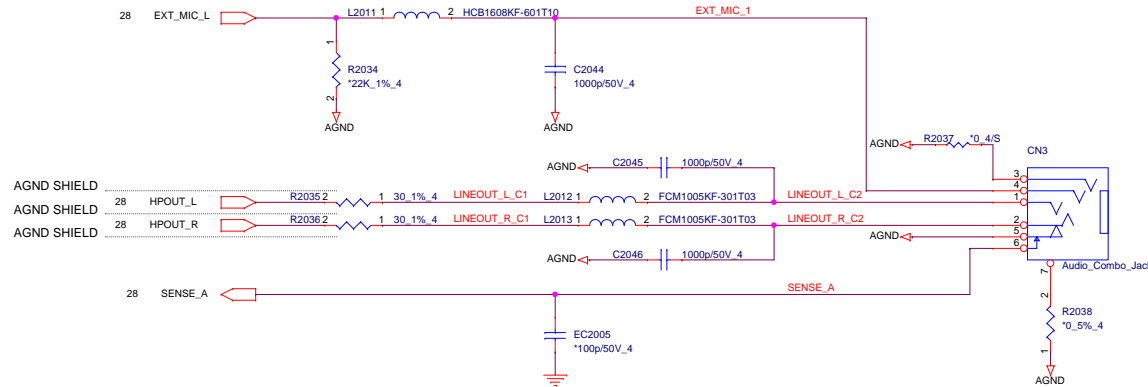
## Close to HDMI connector



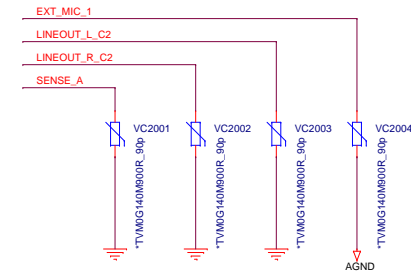
## EMI Solution




## Audio Jack

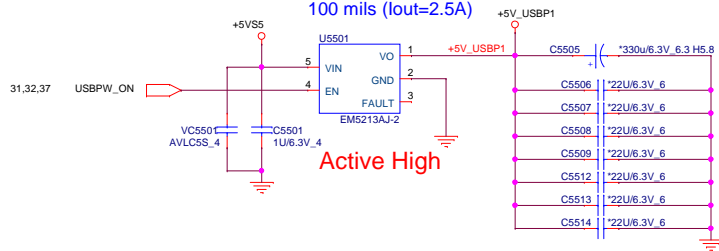


## Audio JACK ESD



 NB5	<b>PROJECT : G74A</b> <b>Quanta Computer Inc.</b>		
	Size C	Document Number <b>30 - LAN RTL8166EH/RTL8111HS</b>	Rev 1A
	Date: Wednesday, January 11, 2017	Sheet 30 of 51	

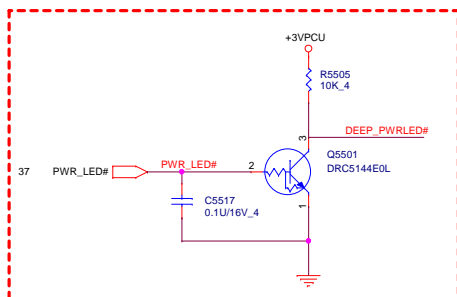
100 mils (Iout=2.5A)



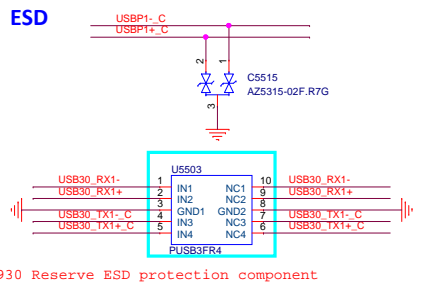
Active High

## Daughter Board

1123 Add PWR\_LED MOS Circuit

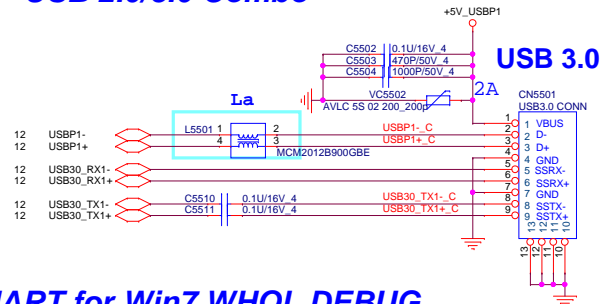


## ESD

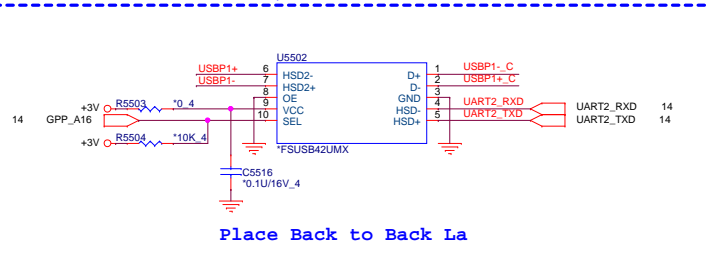


0930 Reserve ESD protection component

## USB 2.0/3.0 Combo



## UART for Win7 WHQL DEBUG

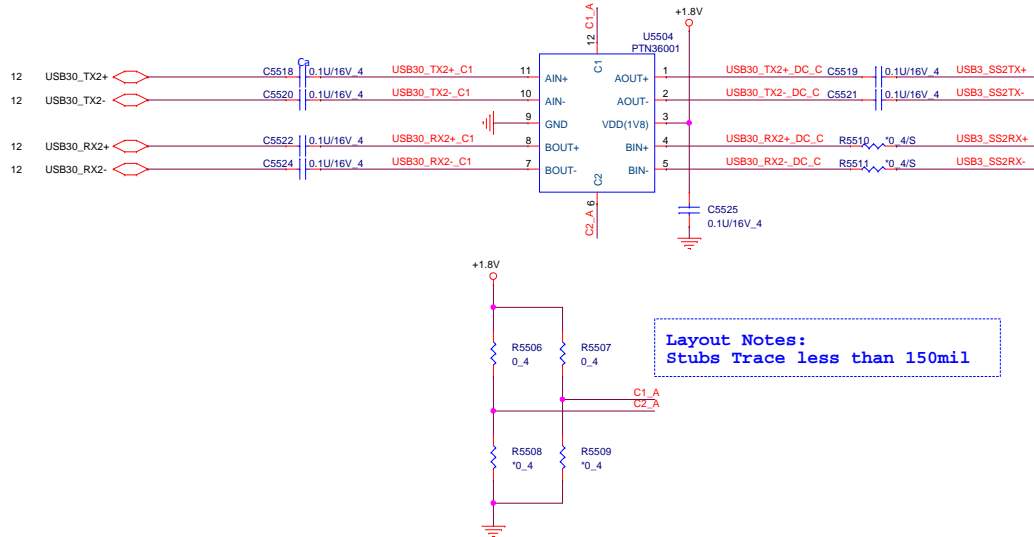


Place Back to Back La

## USB3.0

USB3.0 Re-driver IC

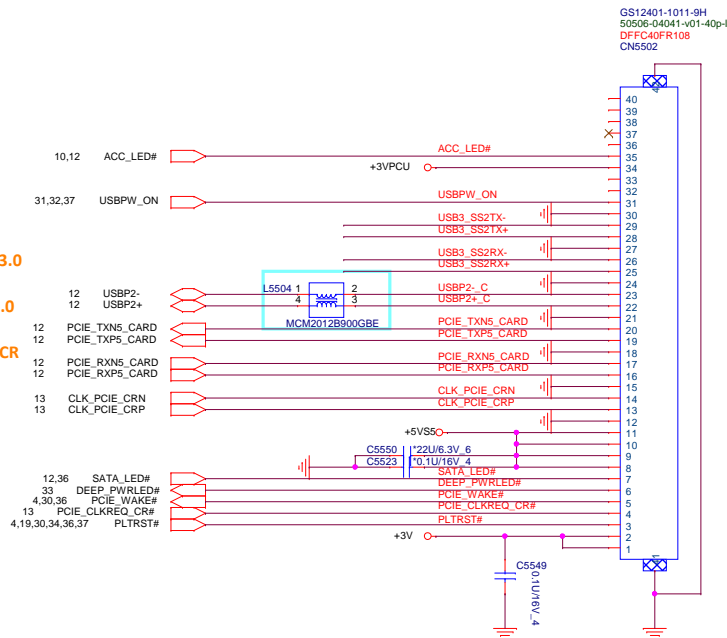
## USB3.0 re-driver IC

Layout Notes:  
Stubs Trace less than 150mil

2 SPD:1 USB3.0

2 SPD :1 USB2.0

15" :PCIE to CR



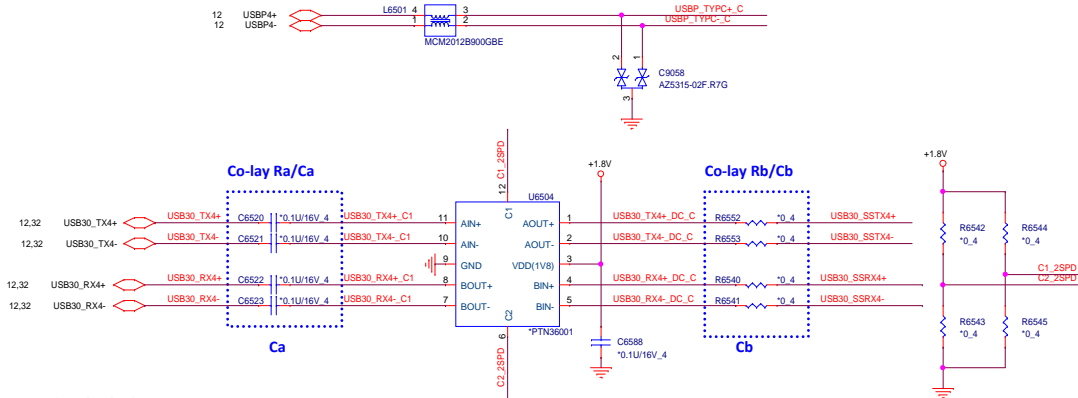
**PROJECT : G74A**  
**Quanta Computer Inc.**

Size Custom Document Number 31 -- USB3.0/DB  
Date: Wednesday, January 11, 2017 Sheet 31 of 51

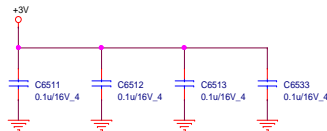
# USB3 SW - EJ179S + USB TYPE-C - TPS25810

32

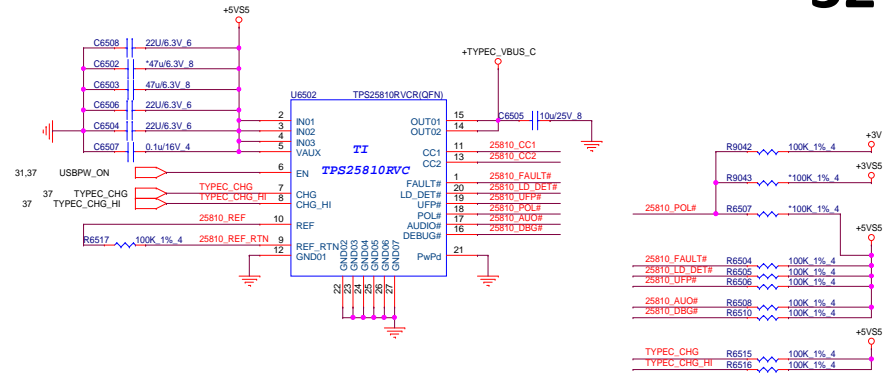
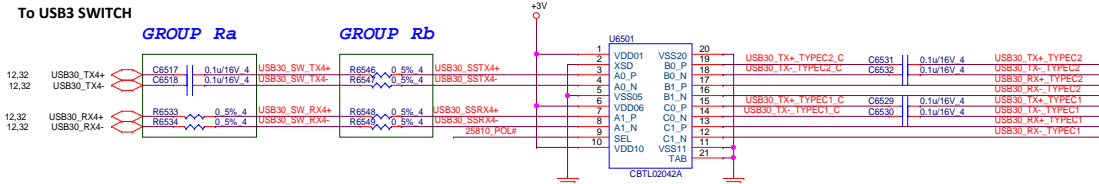
## USB2.0



## USB3.0 SW

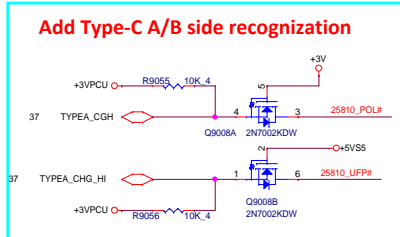
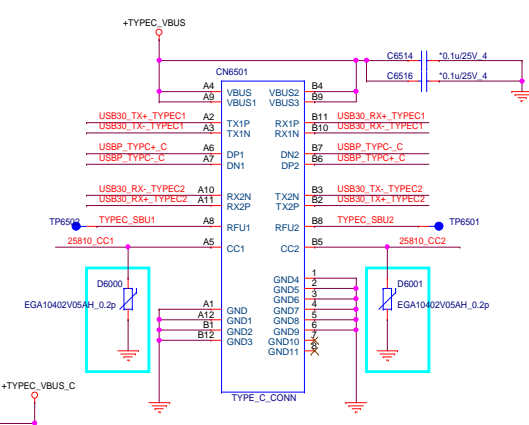


## Differential impedance referenced SOC



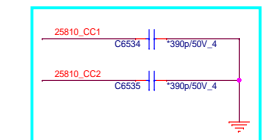
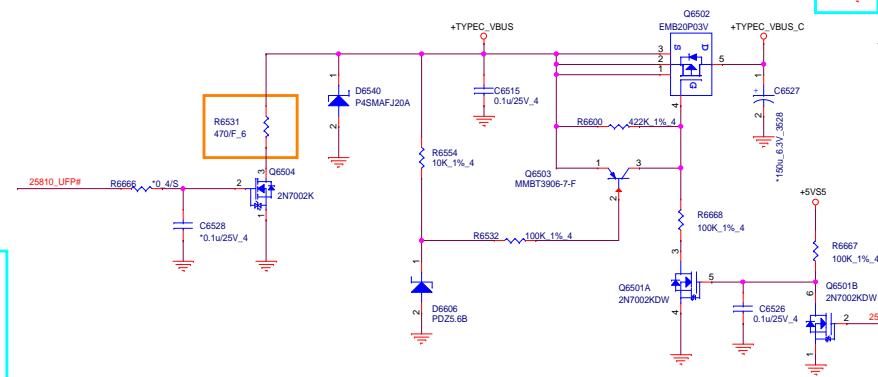
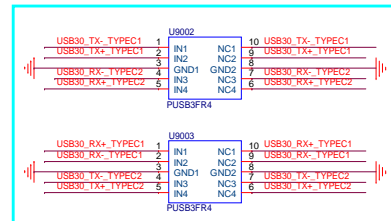
TPS25810 Port	CC1	CC2	OUT	VCONN On CC1 for CC2	POL#	UFP#	AUDID#	DEBUG#
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW	Hi-Z
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

CHG	CHG_H	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	S10	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A



SEL = CMOS single-ended input  
operation mode select  
SEL = LOW: A <----> B  
SEL = HIGH: A <----> C

## TYPE C USB3.0 ESD

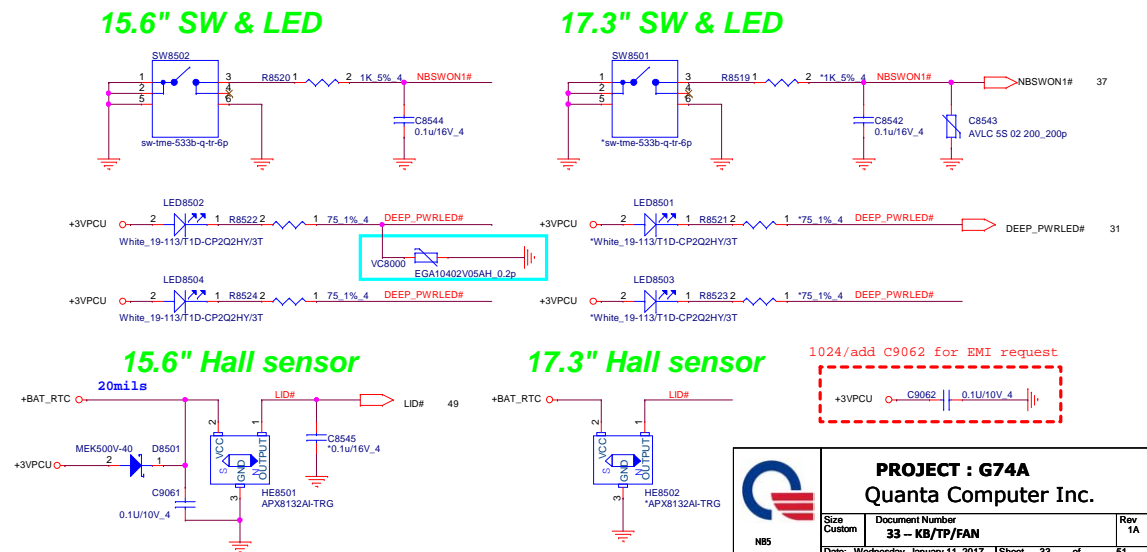




***KB LIGHT CONN***

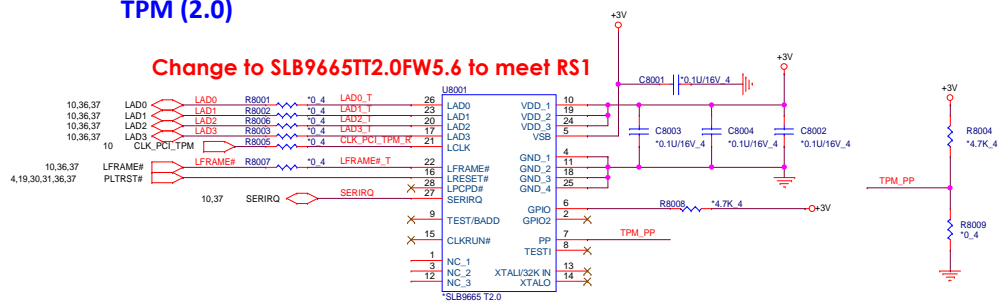


### 17.3" Hall sensor

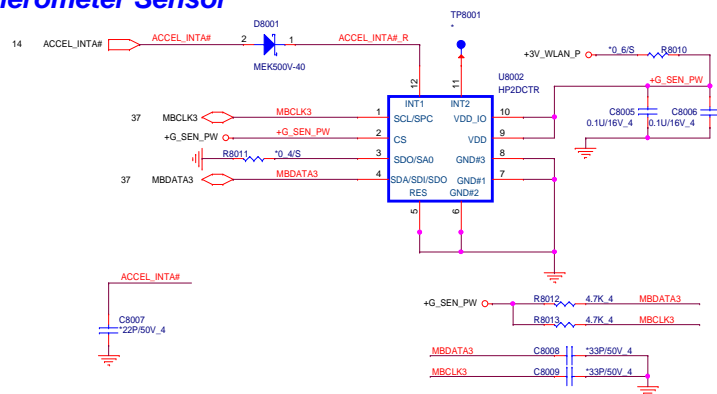


## TPM (2.0)

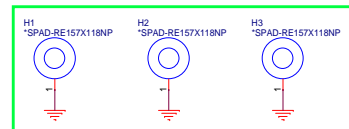
Change to SLB9665TT2.0FW5.6 to meet RS1



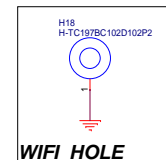
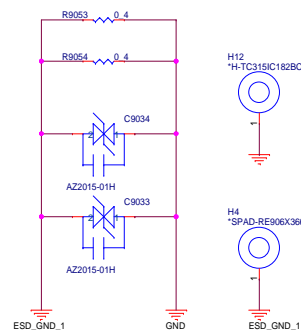
## Accelerometer Sensor



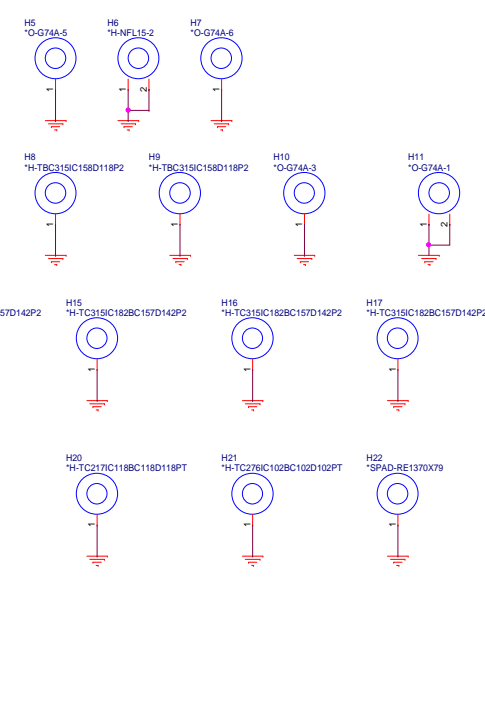
## Holes



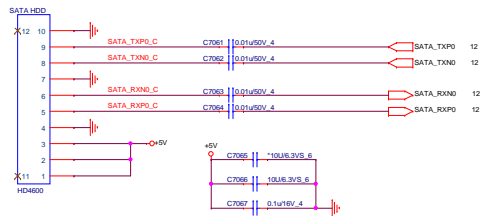
10/17 EMI request



WIFI HOLE



# SATA HDD & LED



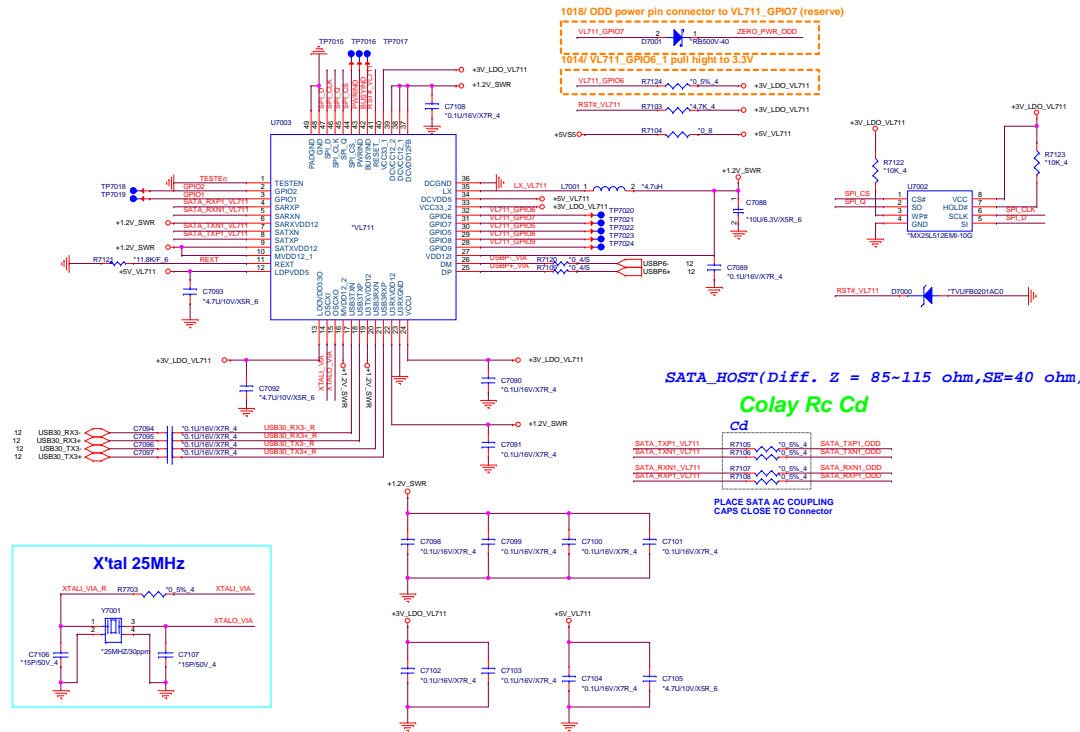
4,28,31,32,39,40,41,42,43,44,46,47,48,51  
24,10,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,36,37,43,46,51

+5V55  
+5V  
+3V



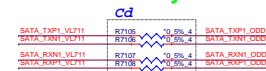
35

# USB3.0 to SATA



SATA\_HOST(Diff. Z = 85-115 ohm,SE=40 ohm)

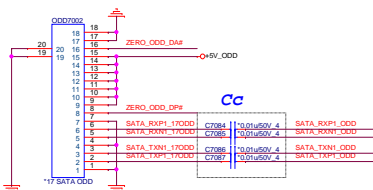
Colay Rc Cd



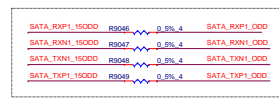
PLACE SATA AC COUPLING CAPS CLOSE TO Connector

# SATA ODD

17.3" ODD

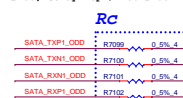


Colay Cc, Ce  
15.6" ODD STUFF



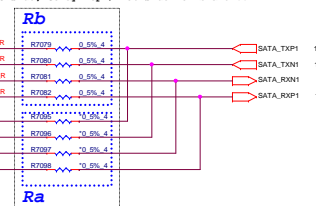
Colay Rc, Cd

Close ODD7001 side, Colay Top / Bot side for branch!!

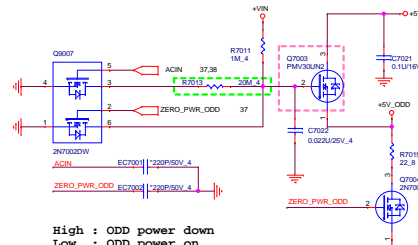
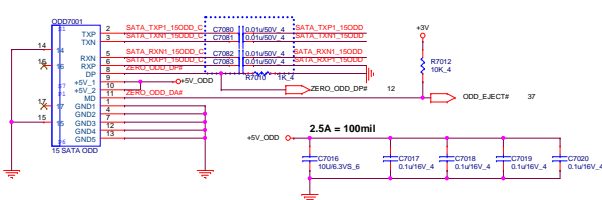


Colay Ra, Rb

Close CPU side, Colay Top / Bot side for branch!!

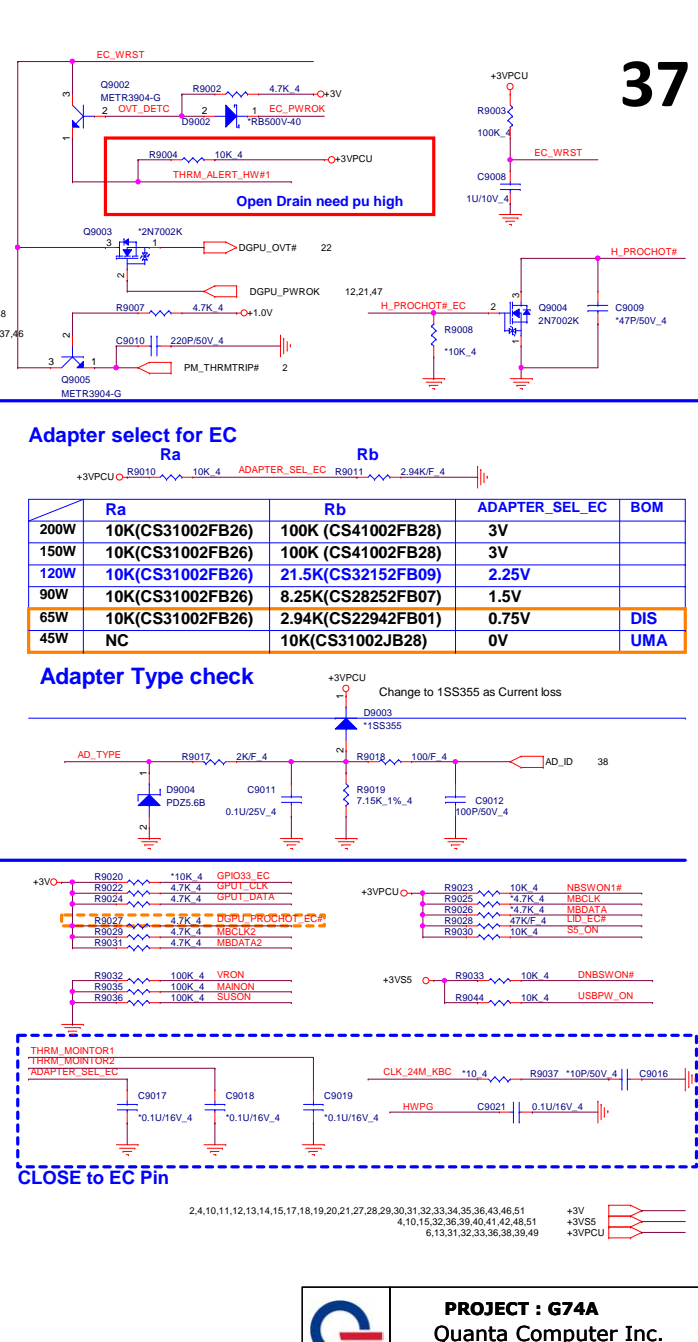


15.6" ODD



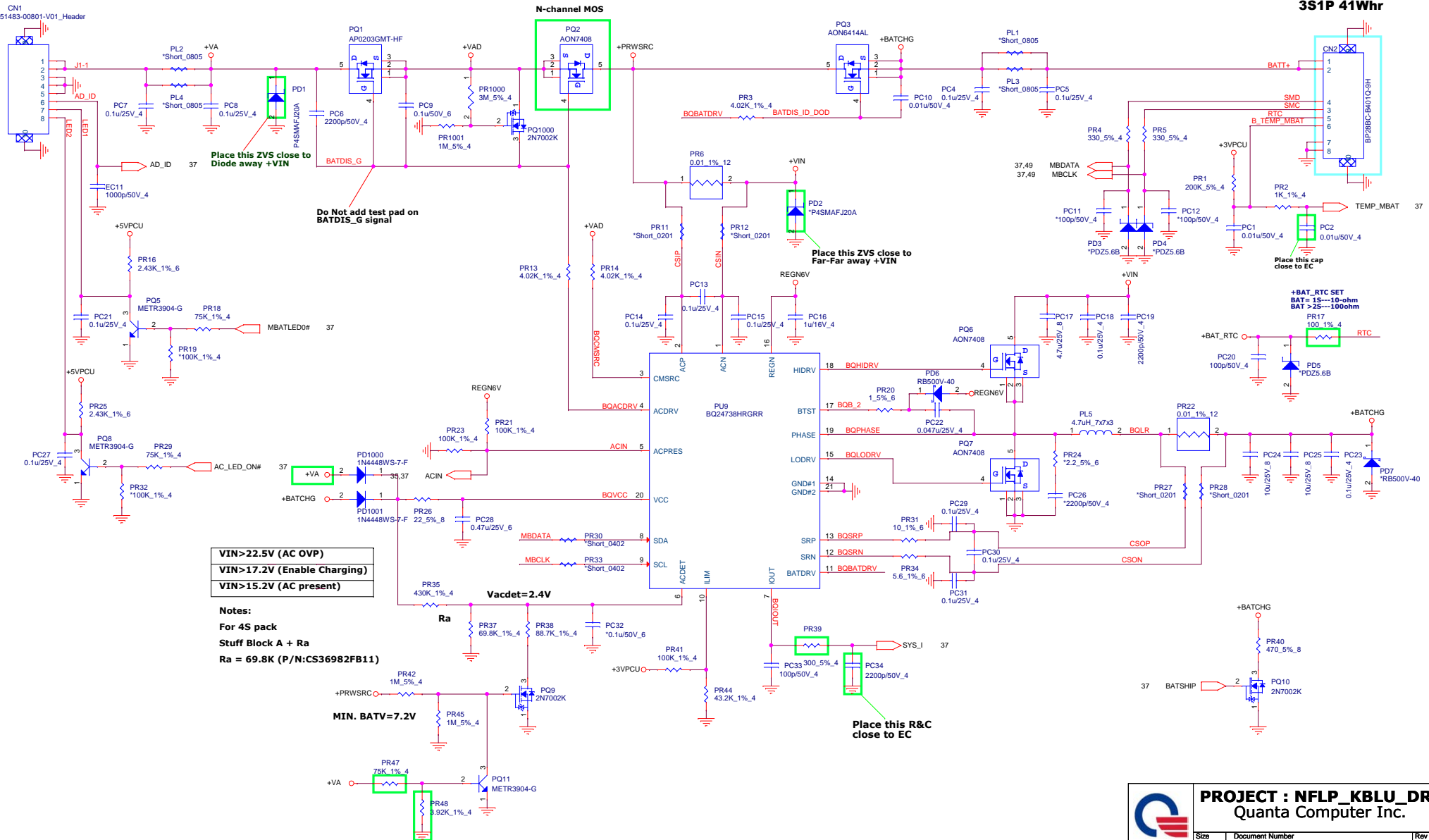
High : ODD power down  
Low : ODD power on



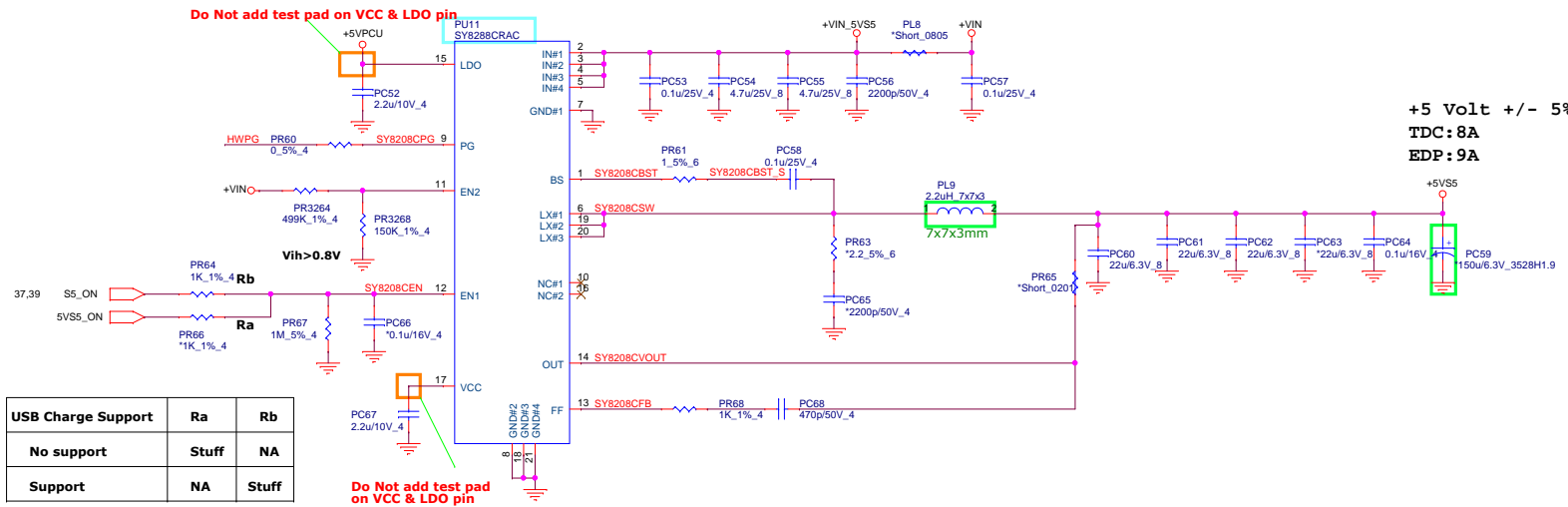
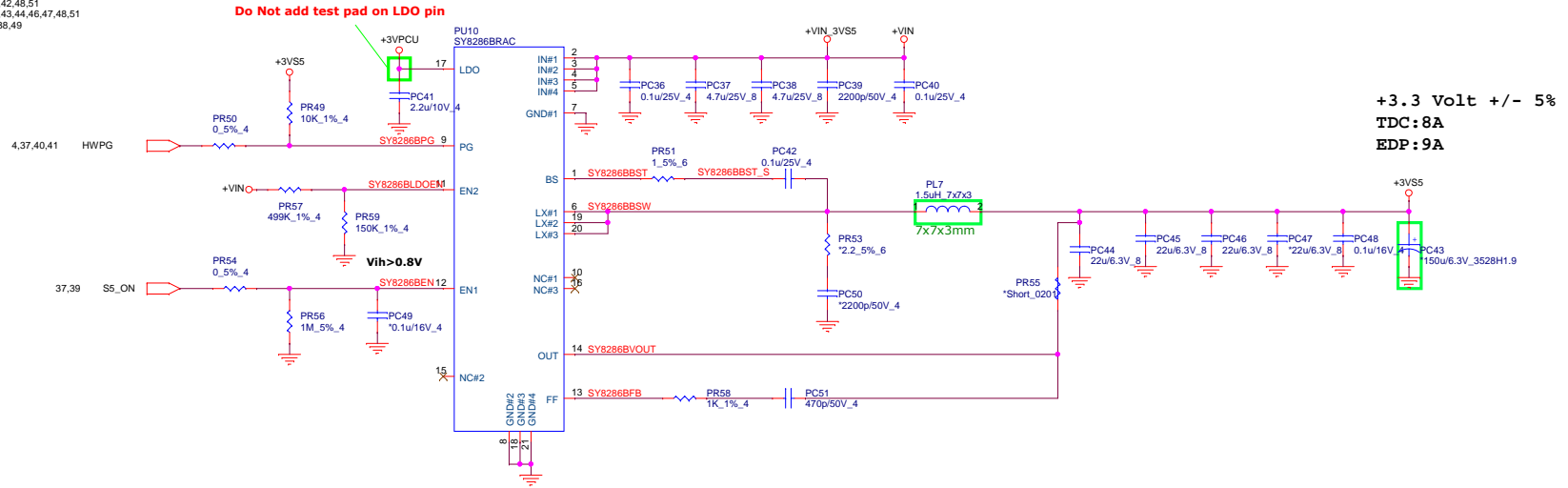


+3VPCU	6,13,31,32,33,36,37,38,39,49
+5VPCU	28,39,48,51
+BAT_RTC	4,13,15,33,49
+VIN	27,33,35,39,40,41,44,45,46,47,50
+3VPCU	6,13,31,32,33,36,37,38,39,49

## ADP=65W

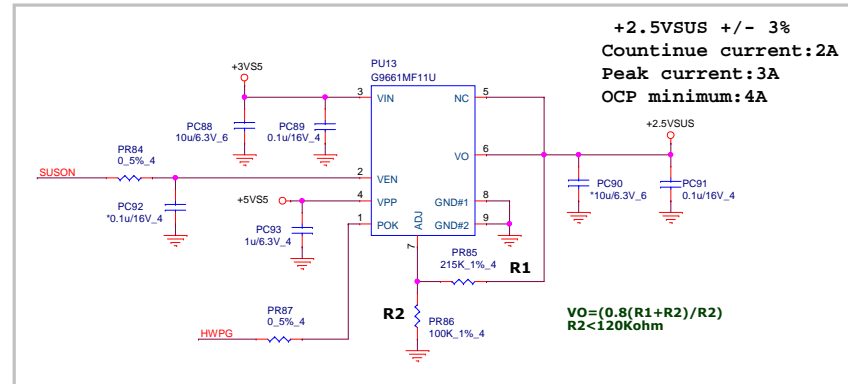
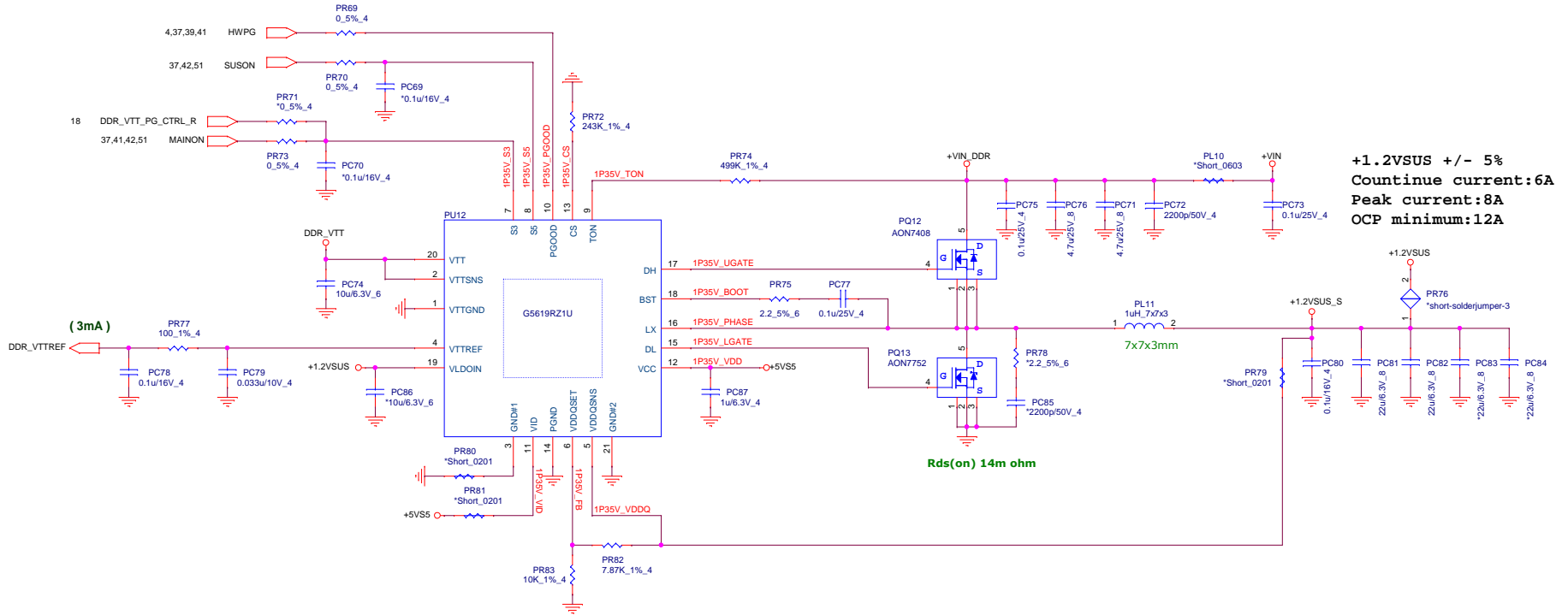


+VIN	27,33,35,38,40,41,44,45,46,47,50
+3VS5	4,10,15,32,36,37,40,41,42,48,51
+5VS5	4,28,31,32,35,40,41,42,43,44,46,47,48,51
+3VPCU	6,13,31,32,33,36,37,38,49
+5VPCU	28,38,48,51



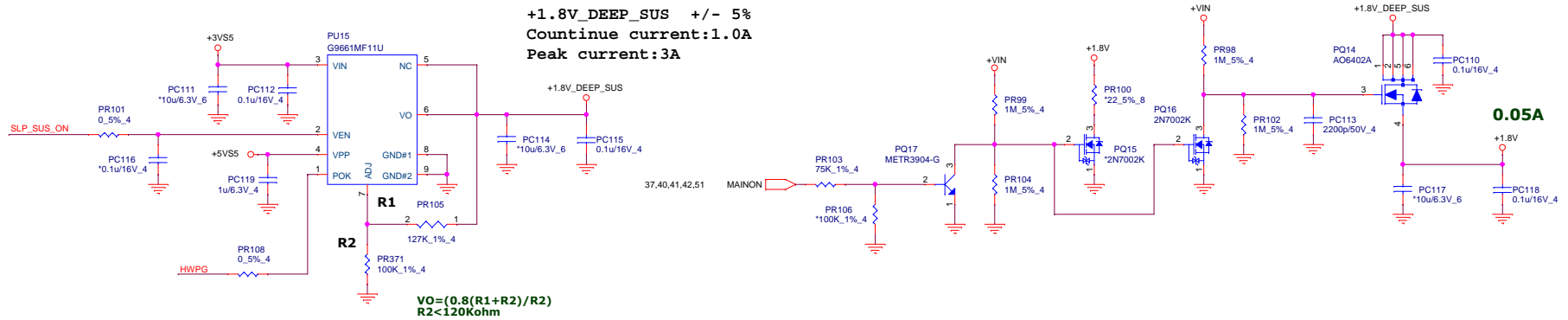
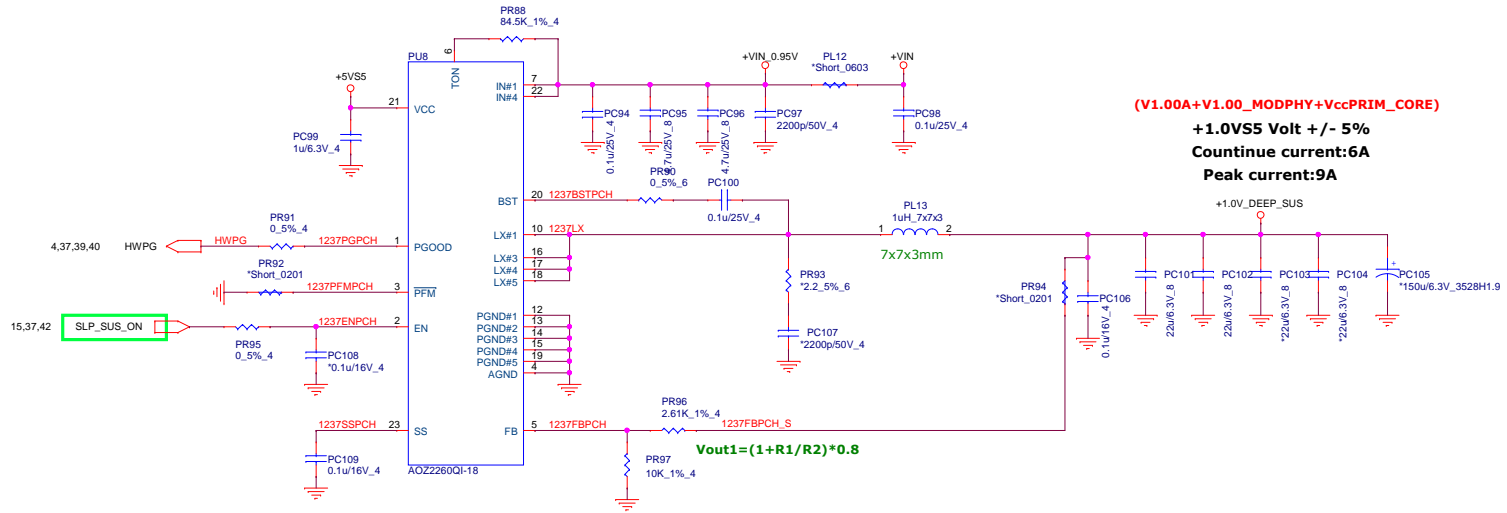
USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

+VIN 27,33,35,38,39,41,44,45,46,47,50  
 +5VS5 4,28,31,32,35,39,41,42,43,44,46,47,48,51  
 +1.2VSUS 3,6,17,18,42,48  
 DDR\_VTT 17,18





+VIN	27,33,35,38,39,40,44,45,46,47,50
+3VS5	4,10,15,32,36,37,39,40,42,48,51
+5VS5	4,28,31,32,35,39,40,42,43,44,46,47,48,51
+1.0V_DEEP_SUS	9,13,15,42
+1.8V_DEEP_SUS	9,15
MAINON	37,40,41,42,51
+1.5V	

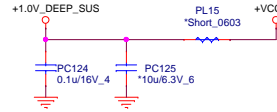


+1.0V	2,4,6,37
+3VSS	4,10,15,32,36,37,39,40,41,48,51
+5VSS	4,28,31,32,35,39,40,41,43,44,46,47,48,51
+VCCIO	2,6
+1.2V_SUS	3,6,17,18,40,48
+VCCSTPLL	2,4,5,6,9,43
+1.0V_DEEP_SUS	9,13,15,41
+1.2V_VCCPLL_OC	6
MAINON	37,40,41,51

**Volume Segment**  
**Vcc\_ST: 0.12A**  
**Vcc\_PLL: 0.12A**

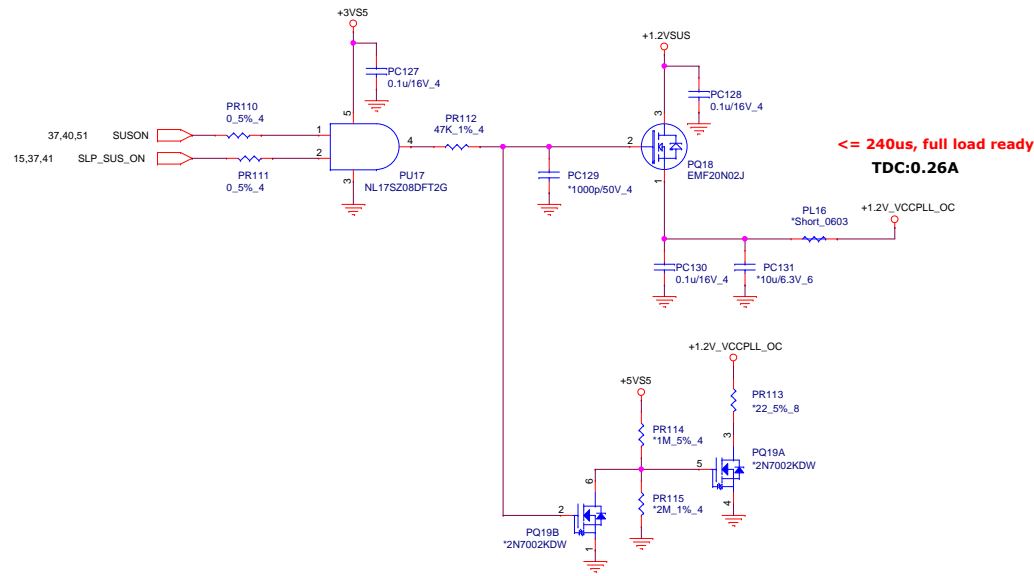
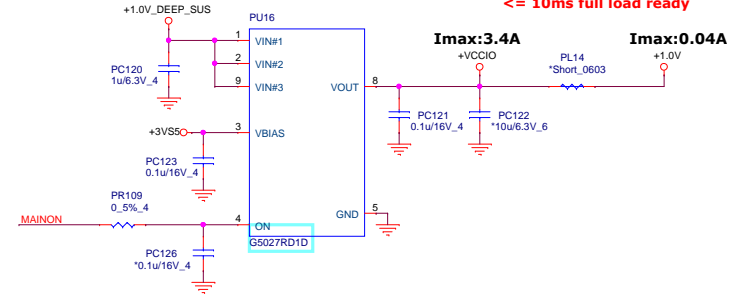
**<= 10ms, full load ready**  
**(Vcc\_ST+Vcc\_PLL)**

**Imax:0.24A**



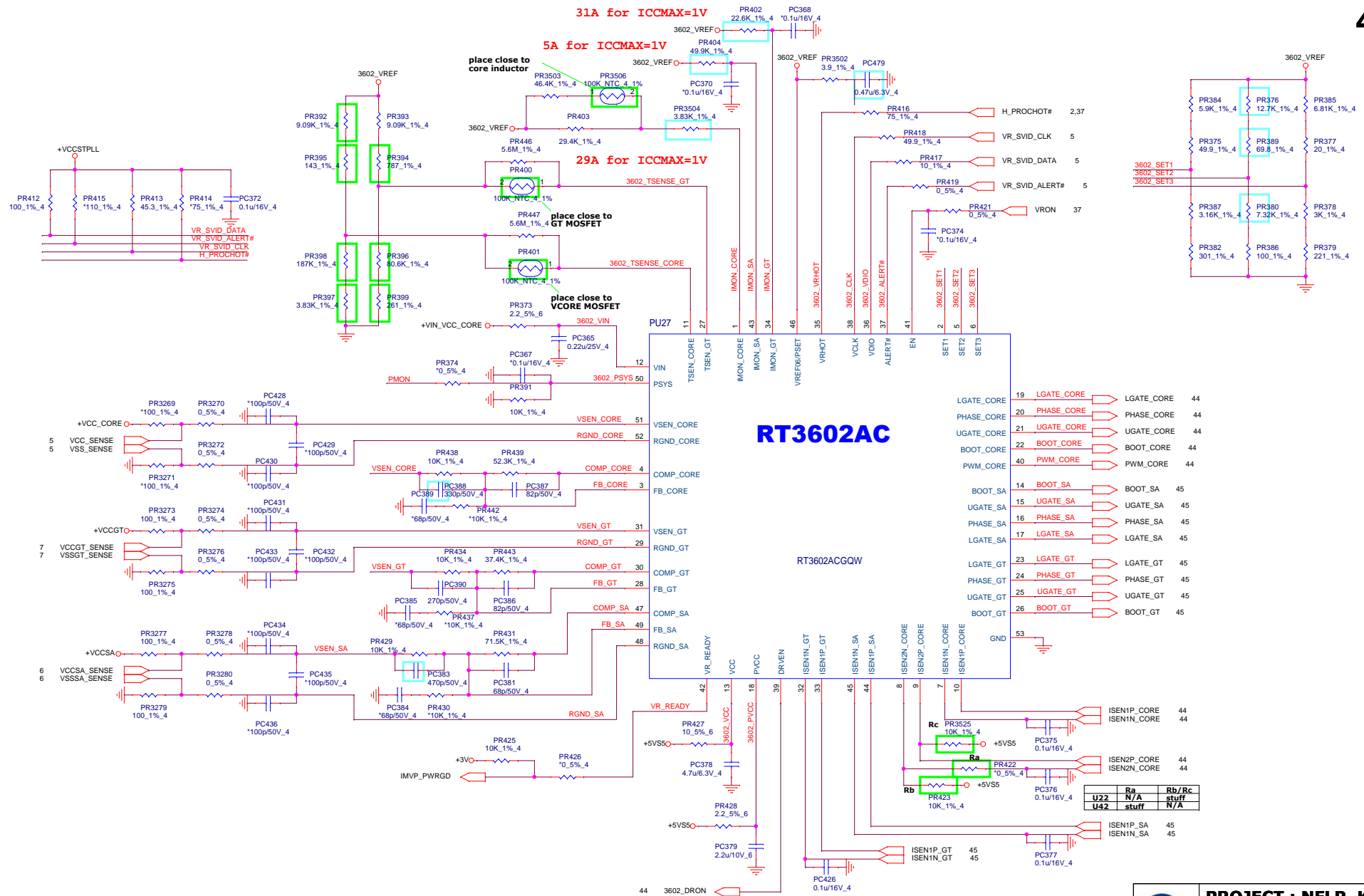
**Volume Segment**  
**Vcc\_STG: 0.04A**  
**Vcc\_IO: 3.4A**

**<= 10ms full load ready**

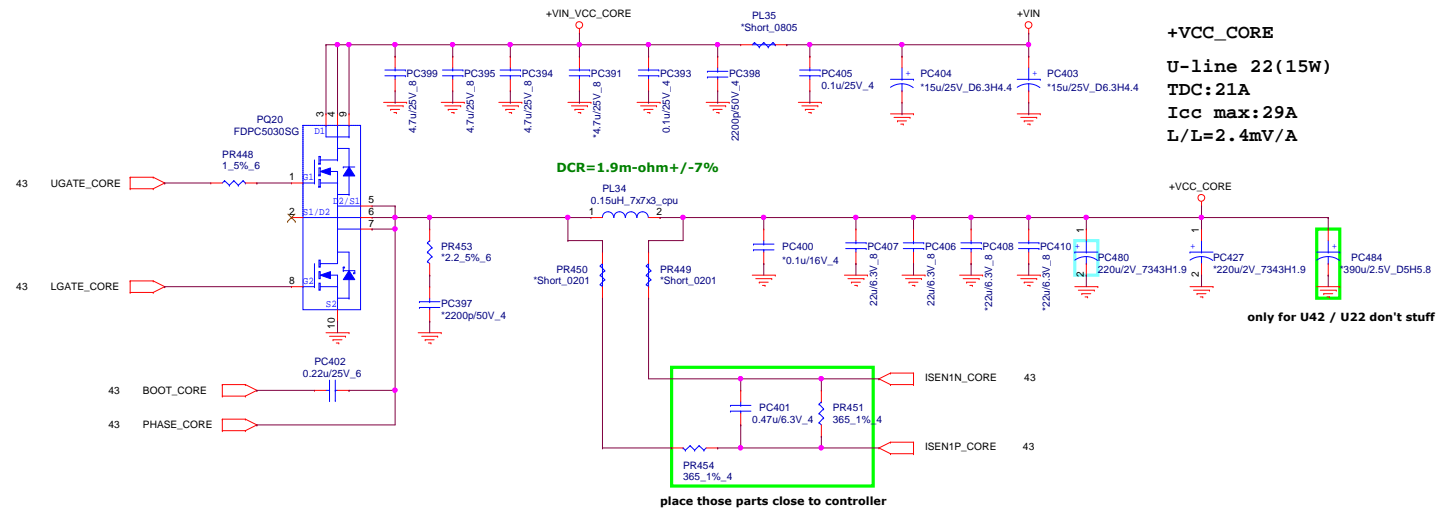


**PROJECT : NFLP\_KBLU\_DR**  
**Quanta Computer Inc.**

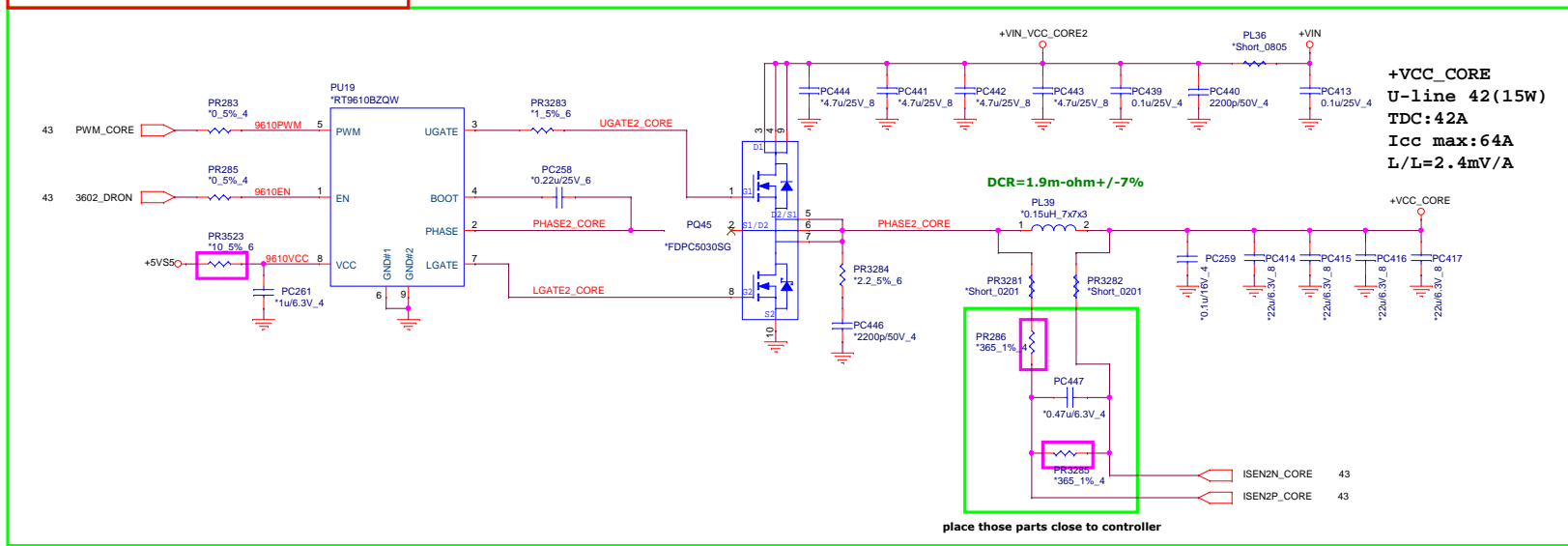
Size Custom	Document Number <b>+1.0V/+VCCSTPLL</b>	Rev 1A
Date: Wednesday, January 11, 2017	Sheet 42 of 51	



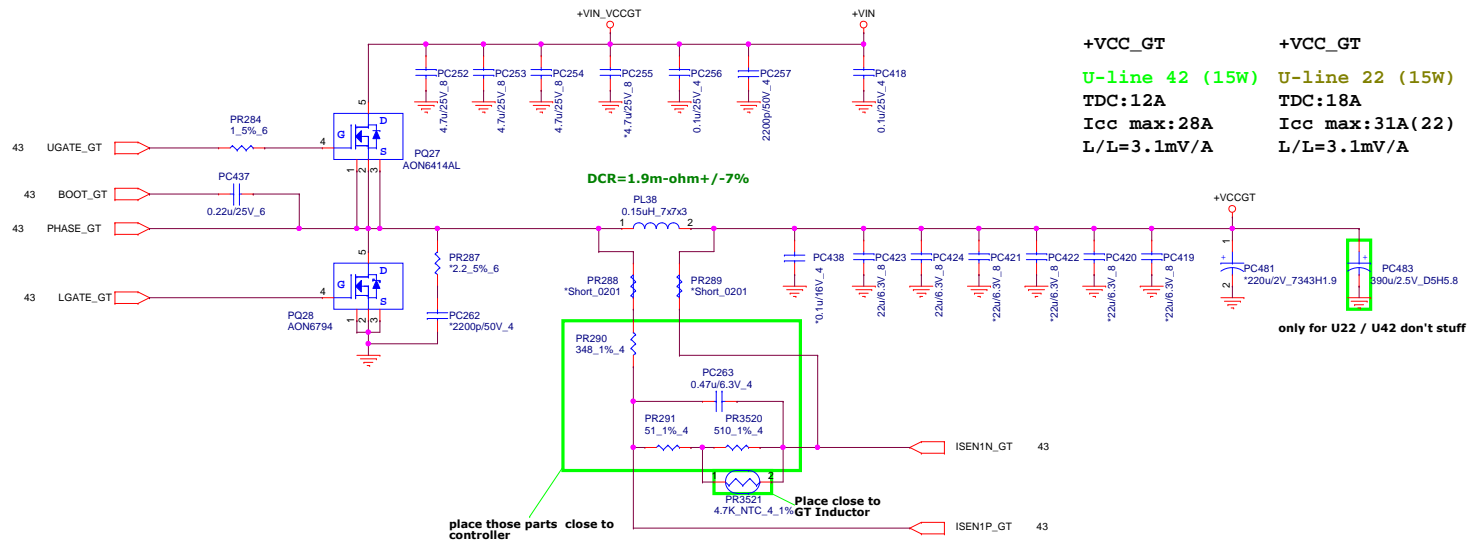
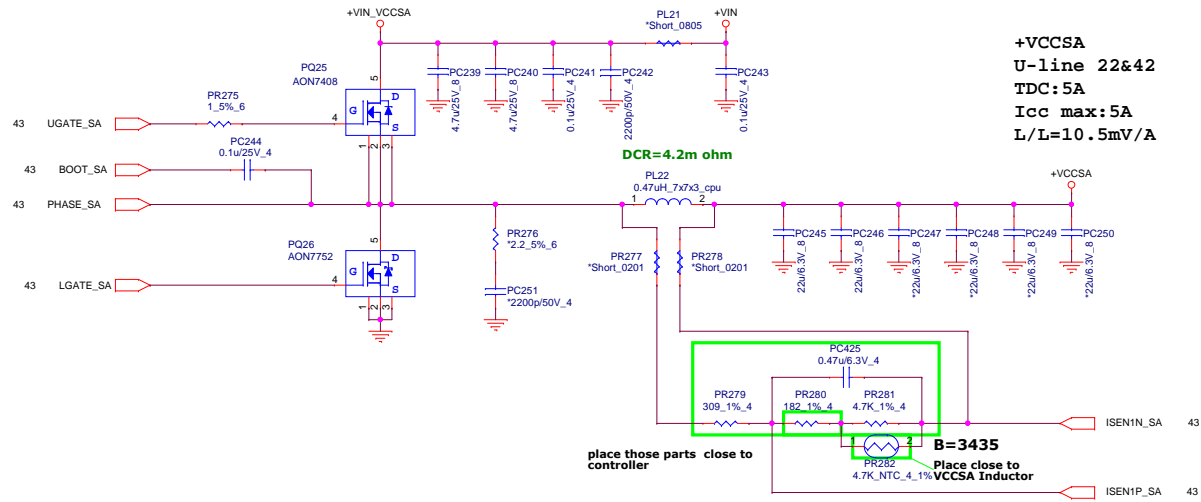
+VIN 27,33,35,38,39,40,41,45,46,47,50  
+5VS5 4,28,31,32,35,39,40,41,42,43,46,47,48,51

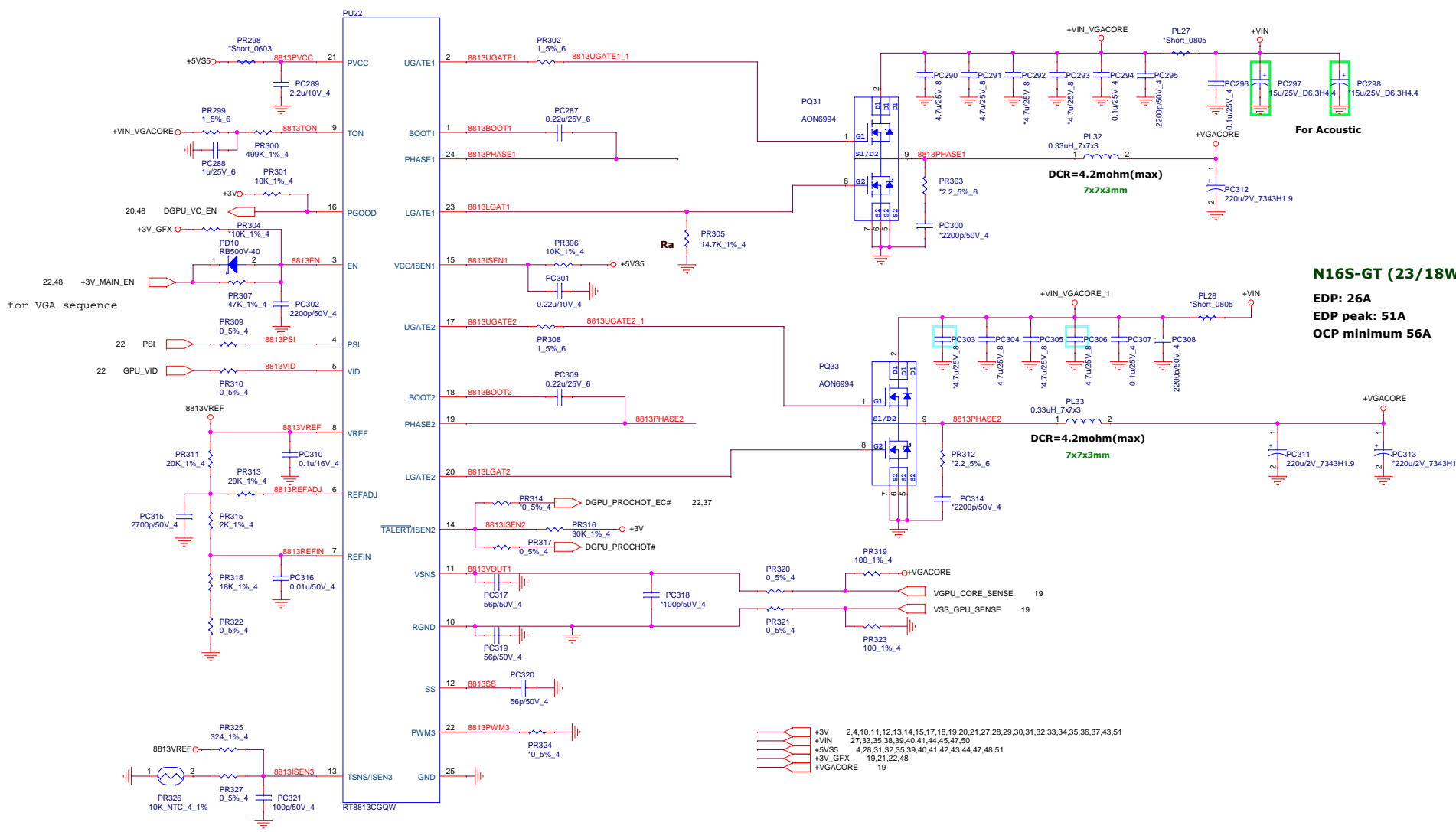


For U42 --> Add These Components



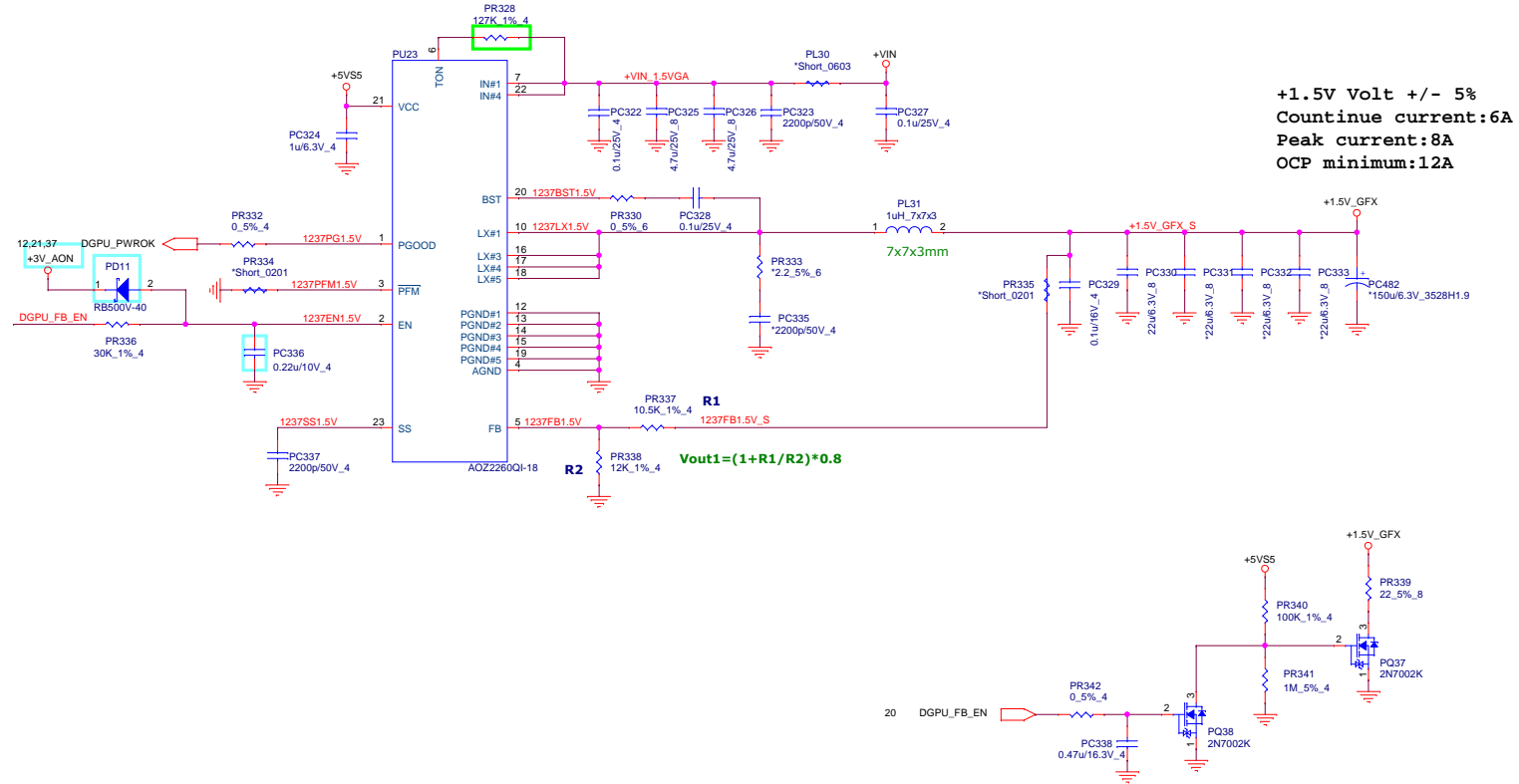
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 +5VSS 4,28,31,32,35,39,40,41,42,43,44,46,47,48,51  
 +VCCSA 6,43  
 +VCCGT 7,43



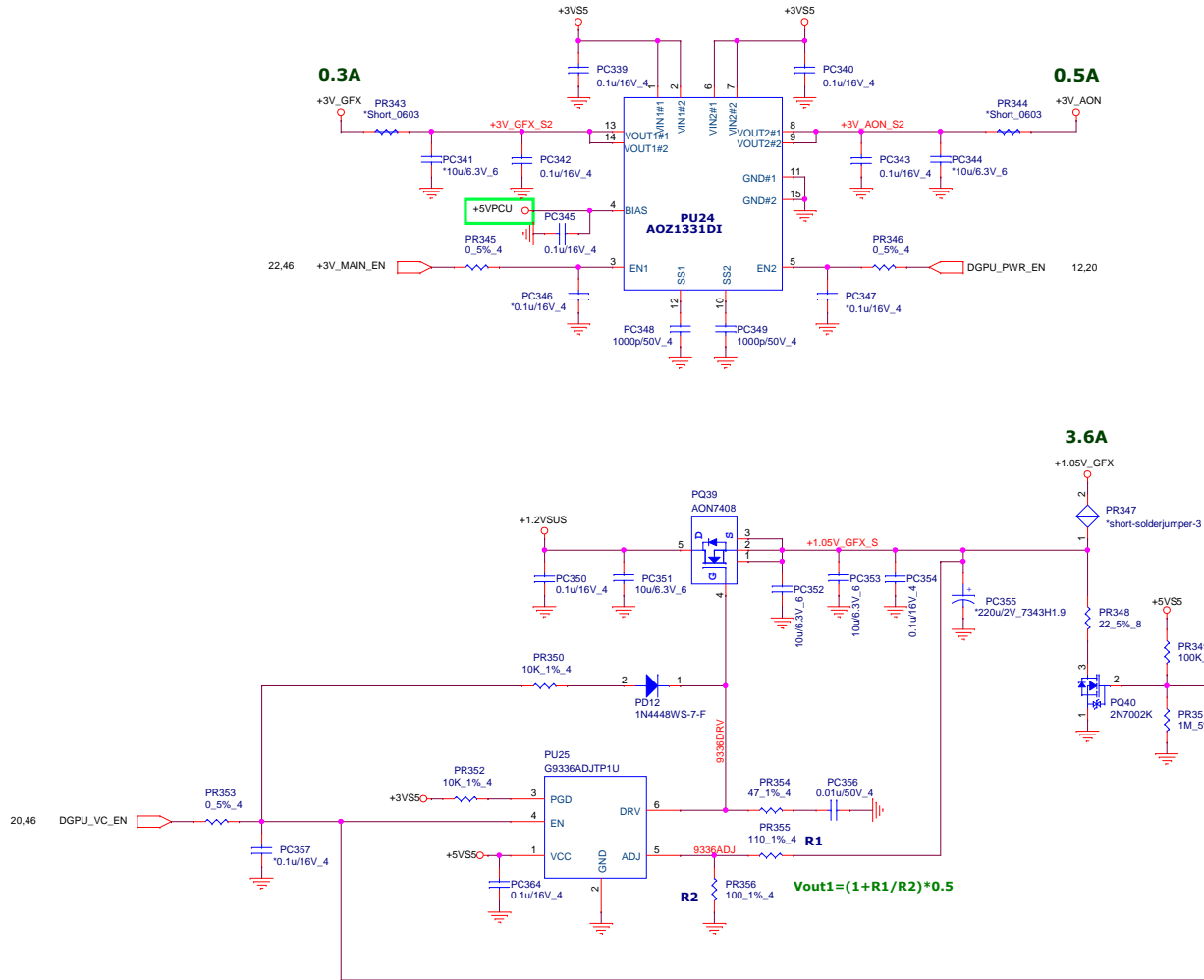


**N16S-GT (23/18W)**  
**EDP: 26A**  
**EDP peak: 51A**  
**OCF minimum 56A**

+VIN 27,33,35,38,39,40,41,44,45,46,50  
 +5VS5 4,28,31,32,35,39,40,41,42,43,44,46,48,51  
 +1.5V\_GFX 20,21,23,24,25,26



+VIN	27,33,35,38,39,40,41,44,45,46,47,50
+3VS5	4,10,15,32,36,37,39,40,41,42,51
+5VS5	4,28,31,32,35,39,40,41,42,43,44,46,47,51
+3V_GFX	19,21,22,46
+3V_AON	19,22,47
+1.2VSUS	3,6,17,18,40,42
+1.05V_GFX	19,20,21

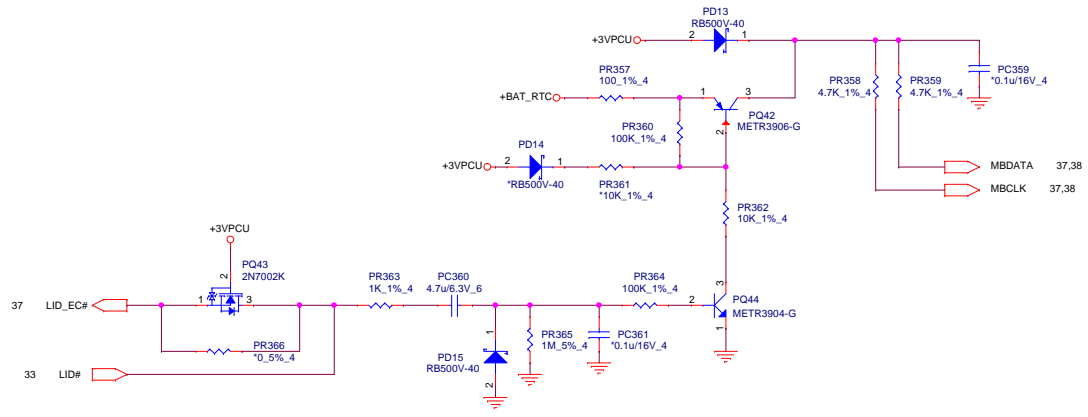


**PROJECT : NFLP\_KBLU\_DR**  
**Quanta Computer Inc.**

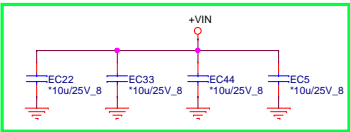
Size	Document Number	Rev
Custom	+3V/+1.05V_GFX(APL3523A)	1A
Date	Wednesday, January 11, 2017	Sheet 48 of 51



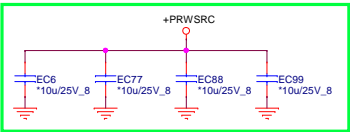
+3VPCU 6,13,31,32,33,36,37,38,39  
+BAT\_RTC 4,13,15,33,38



EMI request for ISN



EMI request for ISN



+3V	2,4,10,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,35,36,37,43,46
+5V	27,28,29,33,35
+VIN	27,33,35,38,39,40,41,44,45,46,47,50
+3VS5	4,10,15,32,36,37,39,40,41,42,48
+5VS5	4,28,31,32,35,39,40,41,42,43,44,46,47,48
+3VSUS	33
+5VPCU	28,38,39,48
+3VLAVCC	30

